ZZZ2
PCB
M/B
DAZ@

ZZZ1
LA-7072P
M/B
DA@

ZZZ3
LS-7072P
LED/B
DA@

ZZZ4
LS-7073P
TP/B
DA@

11/18 ZZZ2 for DAZ P/N:DAZ0IV00101

11/18
LA-7072P P/N from DA60000LA00 to DA60000LA10
LS-7072P P/N from DA40000Z300 to DA40000Z310
LS-7073P P/N from DA40000Z400 to DA40000Z410

11/22
LS-7073P P/N from DA40000Z410 to DA20000Z410

Compal Confidential

P0VE6 LA7072P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

10.1" M/B

2010-11-18

Rev : 1.0

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

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Title: Cover Page

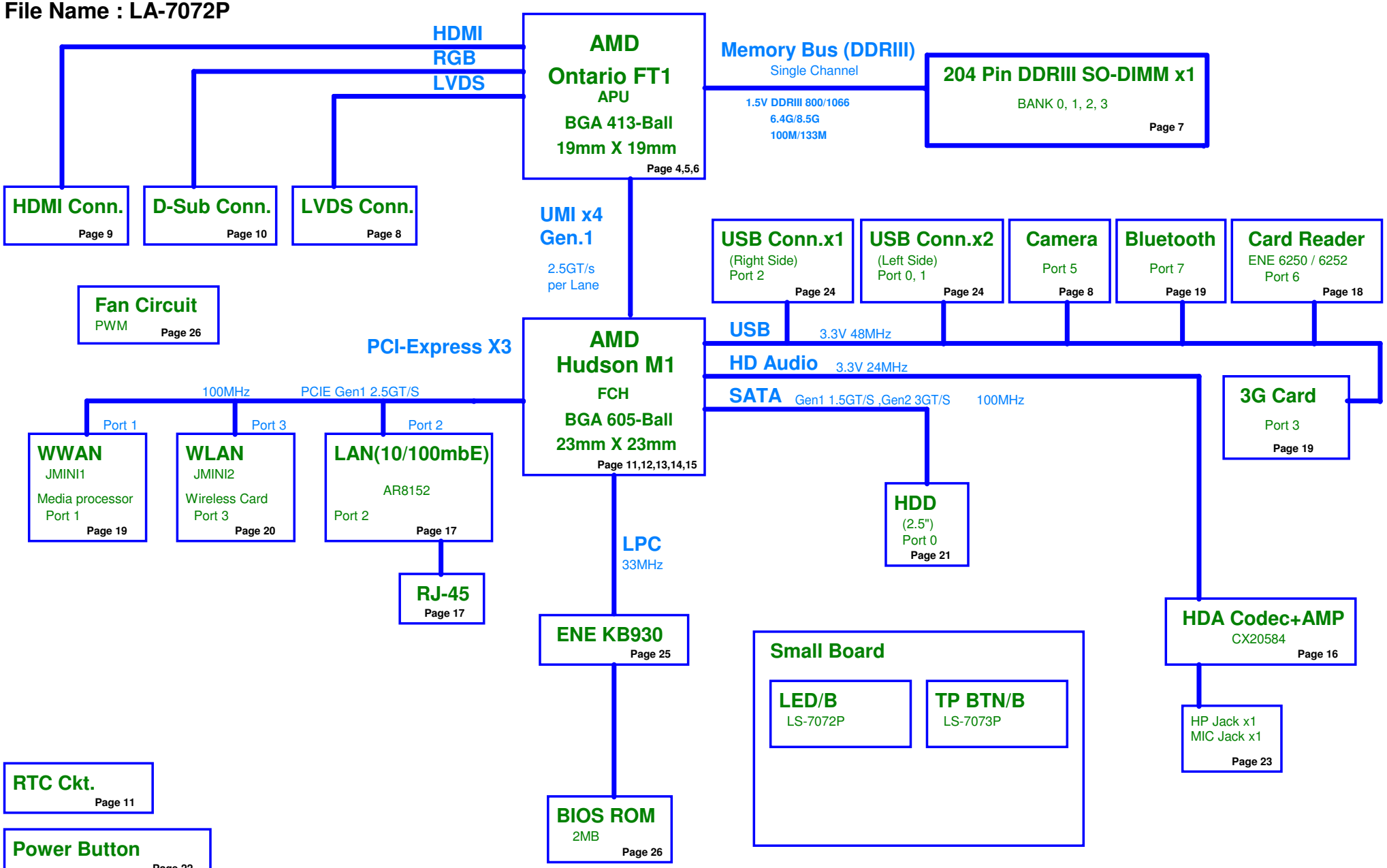
Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Monday, November 22, 2010 | Sheet 1 of 36

Compal Confidential

Model Name : P0VE6 / P0VH6
File Name : LA-7072P

Brazos Platform



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.			
Title	Block Diagrams		
Size B	Document Number P0VE6 Schematics		Rev 1.0
Date: Monday, November 15, 2010	Sheet 2 of 36		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	16H

EC SM Bus2 address

Device	Address	HEX
SB-TSI	1001-100xb	98H

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

BOM Structure

```
 HDMI@ : HDMI function
 BT@   : BT function
 CONN@ : Connetors
 45@   : 45 Level
 3G@   : 3G function
 3G_MP@: 3G & Media processor function
CHARGE@: Charge BATT
NONCHARGE@: nonCharge BATT
```

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Right USB2
Port1	Right USB3
Port2	Left USB1
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	NC
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Board ID / SKU ID Table for AD channel

Vcc	+3VALW
Ra	100K +/- 5%

Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

*

SMBUS Control Table

	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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Issued Date	2010/08/12	Deciphered Date 2012/08/12	Title: Notes List
			Size: B; Document Number: P0VE6 Schematics; Rev: 1.0
			Date: Monday, November 15, 2010; Sheet 3 of 36

R9	R352	Display
mount	@	LVDS
@	mount	eDP

U1

S IC ONTARIO ZMC50AFPB22GT 1G BGA 413P ABO !

SA00004KD40

C50@

10/08 Add U1(C50@) SA00004BM30 S IC ONTARIO ZM101034B2238 1G BGA ABO!

10/08 Change U1 P/N to SA00004DF20 S IC ONTARIO ZM121034B1238 1.2G BGA ABO!

10/27 APU P/N update to B0 stepping

11/03 APU P/N update to SA00004DF60(C30) SA00004BM80(C50)

11/29 Change U1 from SA00004BM80 to SA00004KD40

SA00004DF60

U1B

+1.8VS

R3 1K_0402_5% APU_SVC
R4 1K_0402_5% APU_SVD
R8 510_0402_1% TEST_25_L
R6 1K_0402_5% TEST36

+3VS

R10 10K_0402_5% HDMI_DATA
R11 10K_0402_5% HDMI_CLK
R13 1K_0402_5% APU_PROCHOT#
R14 1K_0402_5% APU_ALERT#_R
R16 1K_0402_5% APU_SIC
R17 1K_0402_5% APU_SID

C405 100P_0402_50V8J LDT_RST#

10/05 Add 100p(C405) on LDT_RST#

Power Circuit

9/9 Change R24 from @ to mount R26 from mount to @

9/15 Change R24 from mount to @

Connection to EC, FCH input need to pull-down

R23 @ 0_0402_5% APU_PROCHOT#
R27 0_0402_5%
R24 @ 0_0402_5% APU_ALERT#_R
R26 @ 0_0402_5%

T9 PAD
T10PAD Close to APU
T14PAD

Power Circuit

R379 0_0402_5%
R380 0_0402_5%

9/6 Add R379, R380 for APU_VDDNB_RUN_FB_L

8/31 Change U1 P/N to SA00004DF00 S IC ONTARIO ZM121034B1238 1.2G BGA 413P

S IC ONTARIO 2M121134B1240 1.2G BGA 413P ABO !

C30@

DISPLAYPORT 1: TDP1_TXP0/TXN0, TDP1_TXP1/TXN1, TDP1_TXP2/TXN2, TDP1_TXP3/TXN3, TDP1_AUXP/AUXN, TDP1_HPD

DISPLAYPORT 0: LTDP0_TXP0/TXN0, LTDP0_TXP1/TXN1, LTDP0_TXP2/TXN2, LTDP0_TXP3/TXN3, LTDP0_AUXP/AUXN, LTDP0_HPD

CLK: CLKIN_H/L, DISP_CLKIN_H/L

SER: SVC/SVD, SIC/SID

CTRL: RESET_L/PWROK, PROCHOT_L, THERMTRIP_L, ALERT_L

JTAG: TDI, TDO, TCK, TMS, TRST_L, DBRDY, DBREQ_L

VDDCR_NB_SENSE, VDDCR_CPU_SENSE, VDDIO_MEM_S_SENSE, VSS_SENSE

RSVD_1, RSVD_2, RSVD_3

DP MISC: DP_ZVSS, DP_BLON, DP_DIGON, DP_VARY_BL

VGA DAC: DAC_RED/REDB, DAC_GREEN/GREENB, DAC_BLUE/BLUEB, DAC_HSYNC/VSYNC, DAC_SCL/SDA, DAC_ZVSS

TEST: TEST4/5/6, TEST14/15/16/17/18/19, TEST25_H/L, TEST28_H/L, TEST31, TEST33_H/L, TEST34_H/L, TEST35/36/37, TEST38 DMAACTIVE_L

8/25 Pull-up 100k(@ R352) to +3VS on LTDP0_HPD for eDP

10/01 Remove T1,T3~T7,T11,T12,T31,T32

9/9 Add R386 (1k@) to +1.8VS on TEST35

9/13 Change R30 from mount to @, R386 from @ to mount (AMD Recommend)

ALLOW_STOP# <11>

R31 1K_0402_5% +1.8VS

+3VS

R32 10K_0402_5% <BOM Structure>
R33 1K_0402_5%
Q1 MMBT3904_NL_SOT23-3
APU_THERMTRIP# H_THERMTRIP# <12>
R34 @ 0_0402_5%

If FCH internal pull-up disabled, level-shifter could be deleted.
Need BIOS to disable internal pull-up!!

2N7002DW-T/R7

Vgs(th): min 1.0V
Typ 1.6V
Max 2.0V

If Q8 or R429, R432 implemented,
EC side pull-up need to be mounted

+3VS

R39 10K_0402_5% @

DMN66D0LDW-7_SOT363-6 Q2A

APU_SID EC_SMB_DA
R47 @ 0_0402_5% FCH_SID FCH_SID <12> T0 FCH
R48 0_0402_5% EC_SMB_DA2 EC_SMB_DA2 <25> TO EC
R49 0_0402_5%

8/19 Change Q2A Q2B SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

DMN66D0LDW-7_SOT363-6 Q2B

APU_SIC EC_SMB_CK
R50 @ 0_0402_5% FCH_SIC FCH_SIC <12> T0 FCH
R51 0_0402_5% EC_SMB_CK2 EC_SMB_CK2 <25> TO EC
R52 0_0402_5%

9/17 Remove JHDT1 R40, R44, R45, R46 , Add T26~T32

AMD Debug

9/20 Delete R41~R43

+1.8VS

R37 1K_0402_5% APU_TRST#

T29PAD
T30PAD

APU_TCK R35 1K_0402_5%
APU_TMS R36 1K_0402_5%
APU_TDI R38 1K_0402_5%
APU_TDO
APU_PWRGD R5 300_0402_5%
LDT_RST# R7 300_0402_5%
APU_DBRDY
APU_DBREQ# R2 300_0402_5%

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Title: FT1 CTRL/DP/CRT

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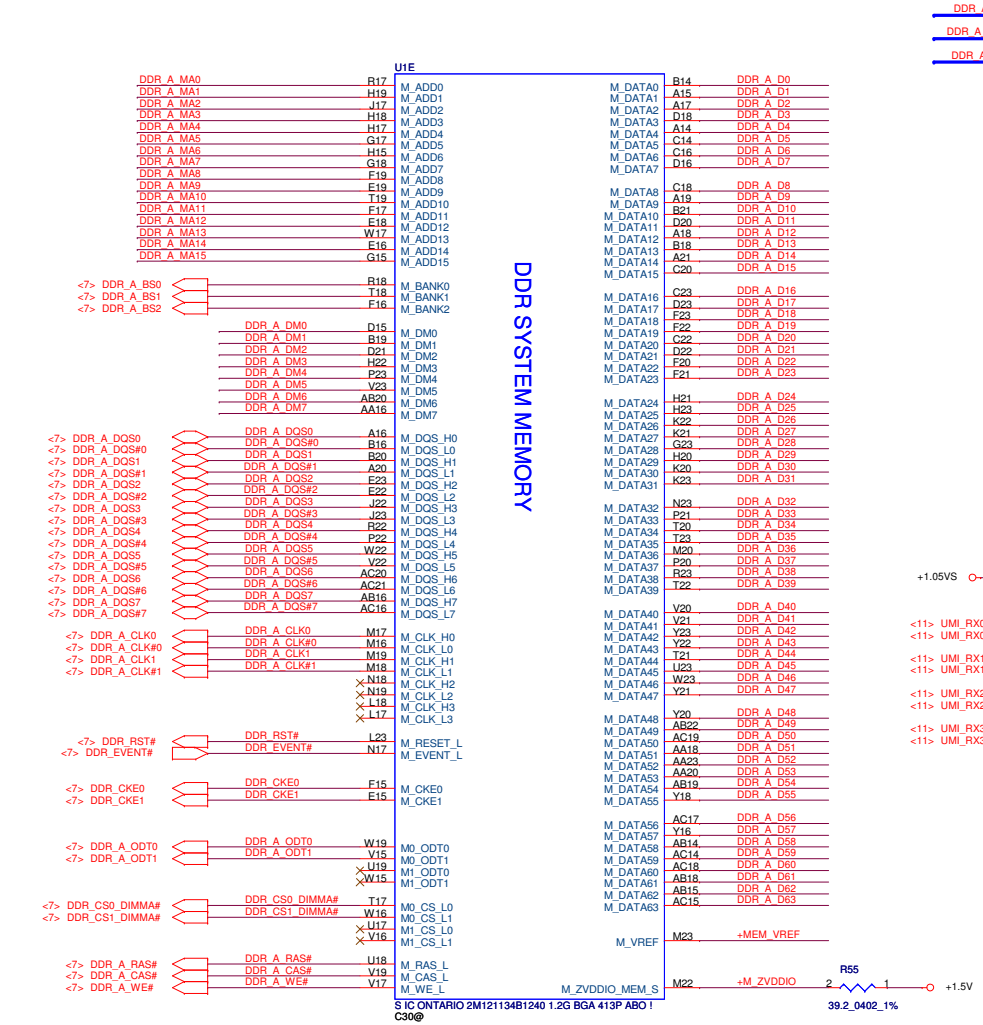
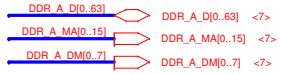
Date: Monday, November 29, 2010 | Sheet 4 of 36



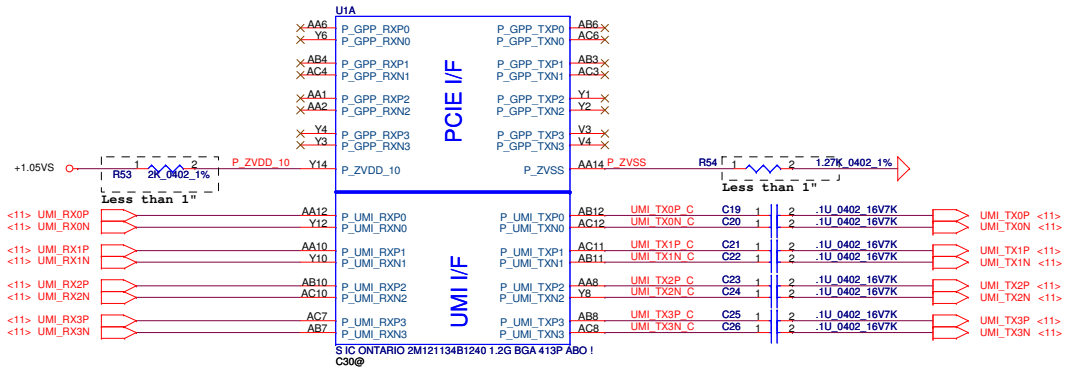


8/22 Delete C11~C18 (No VGA)

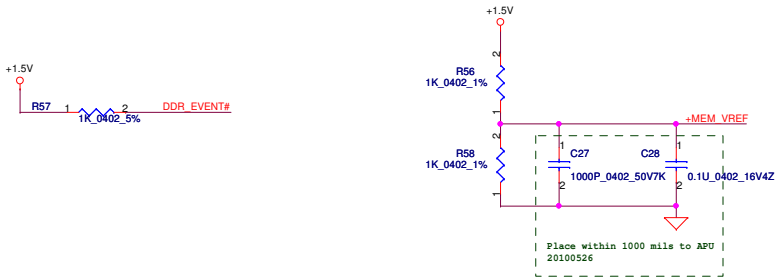
9/6 Change PCI-E from FCH to APU

9/6 Update PCI-E port List

9/15 Change PCI-E from APU to FCH



9/11 Delete DDR Signal link to JDIMM2



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Issued Date	2010/08/12	Deciphered Date	2012/08/12

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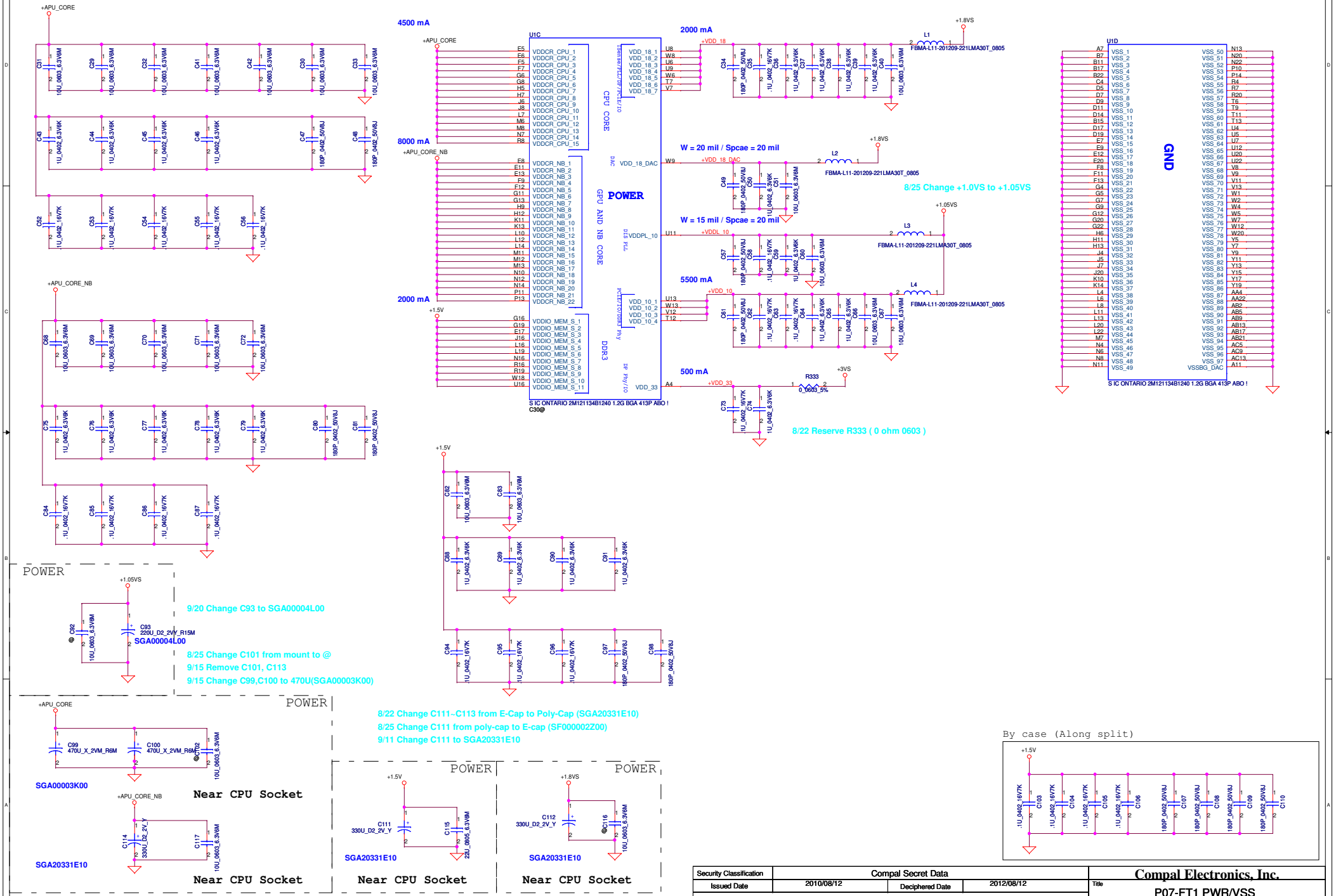
Title: FT1 DDRIII/UMI/PCIE

Size	Document Number	Rev
Custom	P0VE6 Schematics	1.0

Date: Wednesday, November 17, 2010 | Sheet 5 of 36



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Issued Date	2010/08/12	Deciphered Date	2012/08/12

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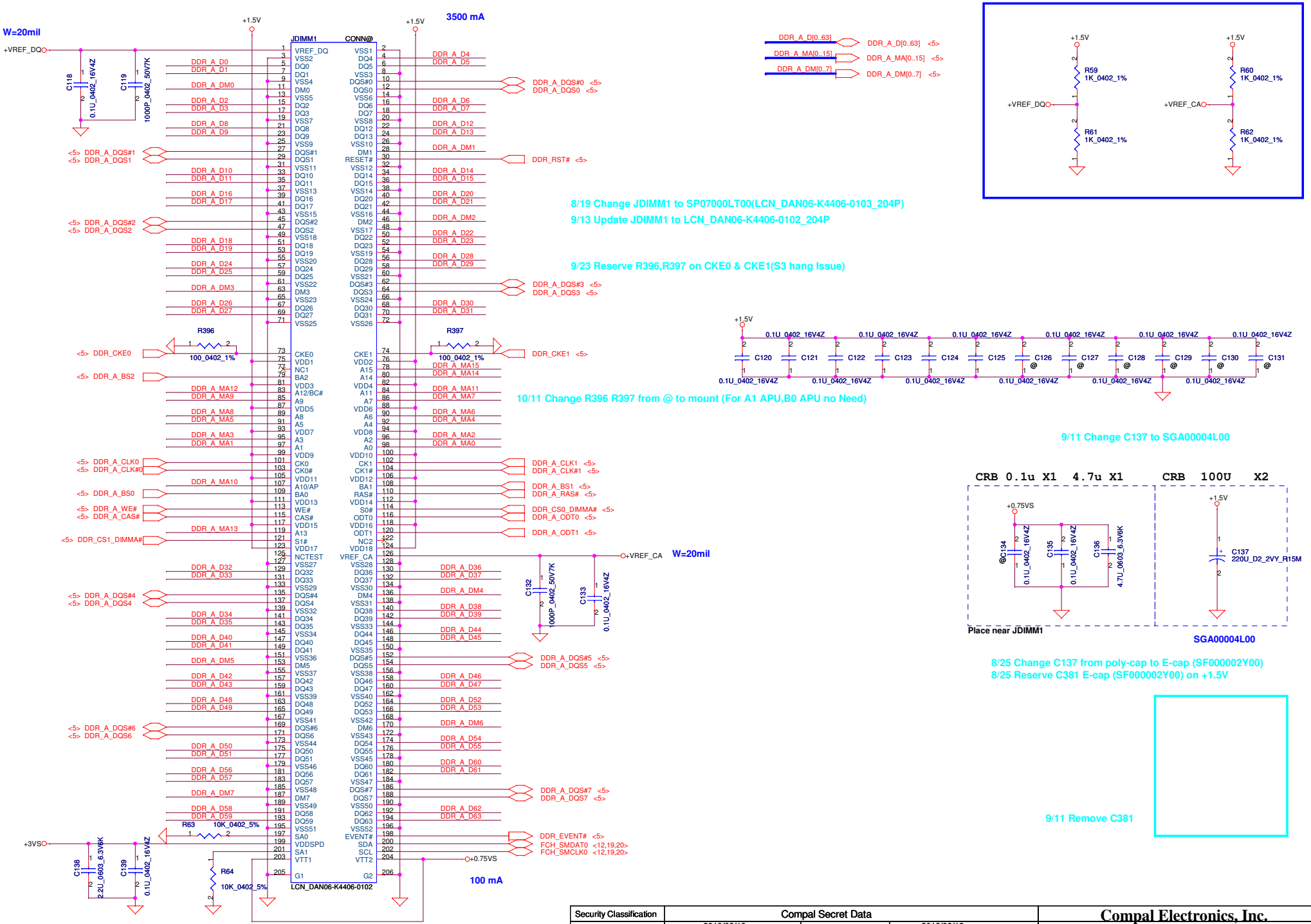
Compal Electronics, Inc.

Title: P07-FT1 PWR/VSS

Size	Document Number	Rev
C	P0VE6 Schematics	1.0

Date: Wednesday, November 17, 2010 Sheet 6 of 36



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: DDR3 SODIMM-I Socket

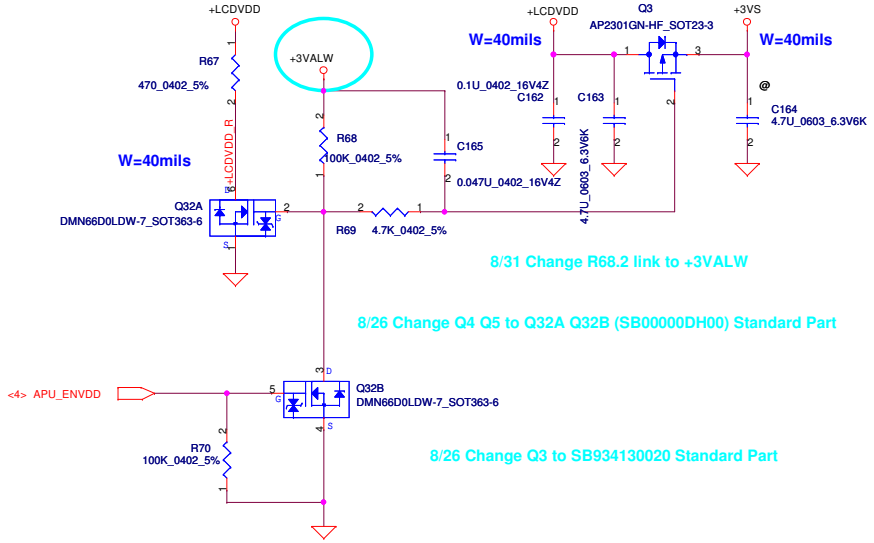
Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 7 of 36

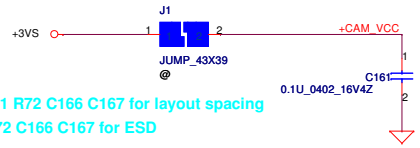
LCD POWER CIRCUIT

9/24 Change Q3 to SB000007H10

11/02 Change Q3 PN to SB934130020



About Camera

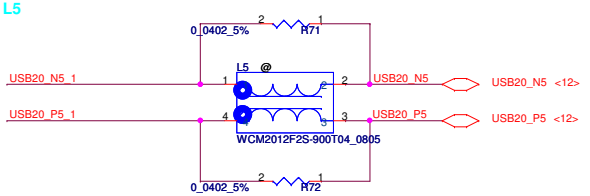


9/15 Remove D1 L5 R71 R72 C166 C167 for layout spacing

9/23 Add D1 L5 R71 R72 C166 C167 for ESD

9/23 Remove D1 C166 C167

9/24 Swap L5



9/9 Reserve 100k PD to GND on INVTPWM

9/17 Change R387 from @ to mount

CMOS & LCD/PANEL BD. Conn.

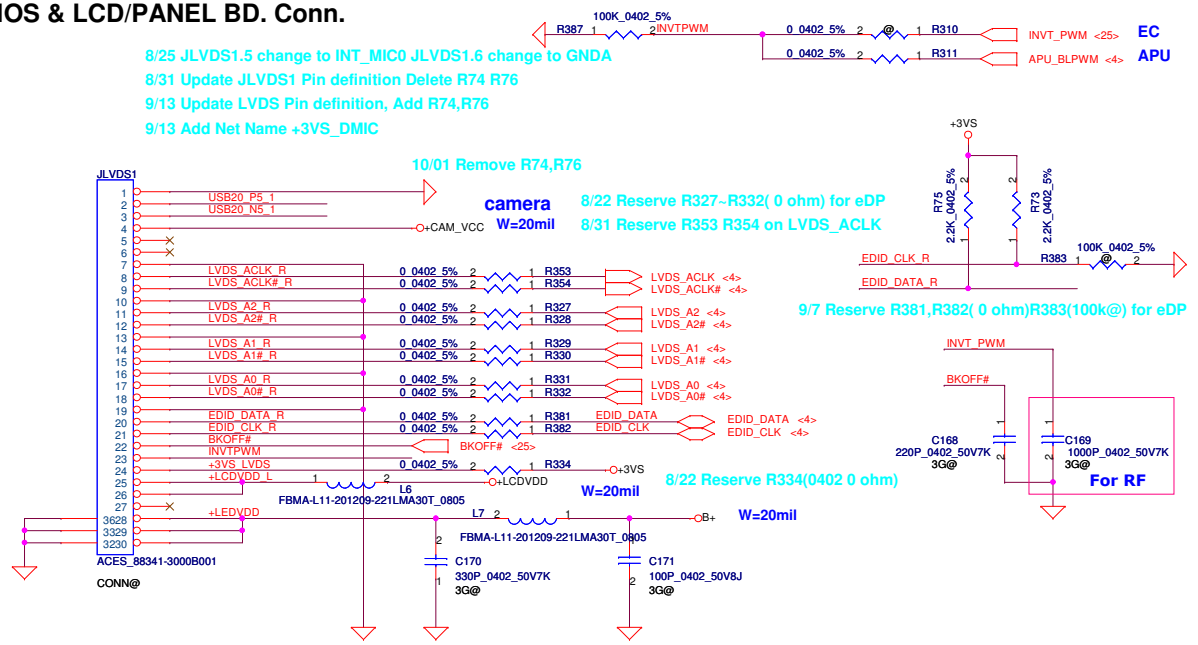
8/25 JLVDS1.5 change to INT_MIC0 JLVDS1.6 change to GNDA

8/31 Update JLVDS1 Pin definition Delete R74 R76

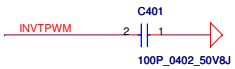
9/13 Update LVDS Pin definition, Add R74,R76

9/13 Add Net Name +3VS_DMIC

10/01 Remove R74,R76



10/04 Add 100p(C401) on INVT_PWM

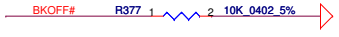


10/04 Change C401 on INVTPWM

*

Display	LVDS	eDP
R331	0 ohm	0.1uF
R332	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

9/3 Pull-Down 10k(R377) to GND on BKOFF#



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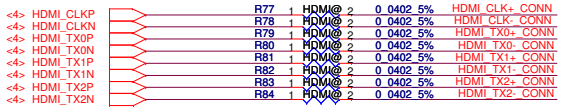
Issued Date	2010/08/12	Deciphered Date	2012/08/12

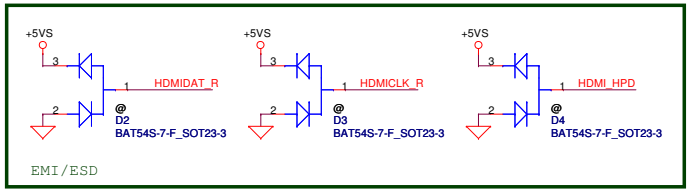
Compal Electronics, Inc.

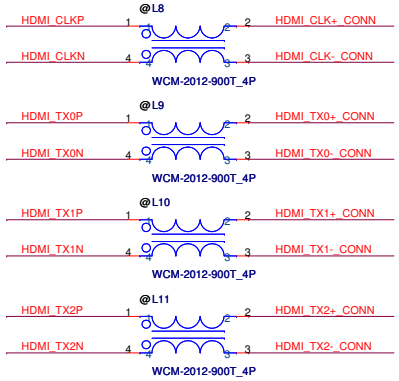
Title: LVDS / Camera

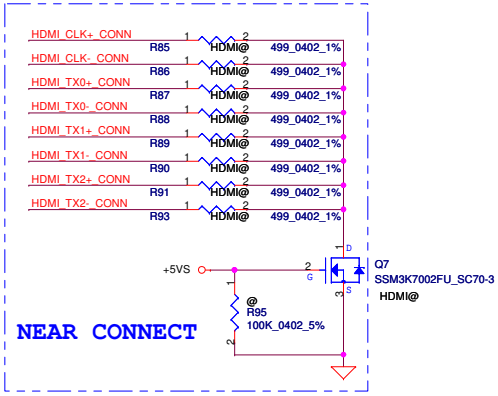
Size	Document Number	Rev
B	P0VE6 Schematics	1.0

Date: Wednesday, November 17, 2010 | Sheet 8 of 36

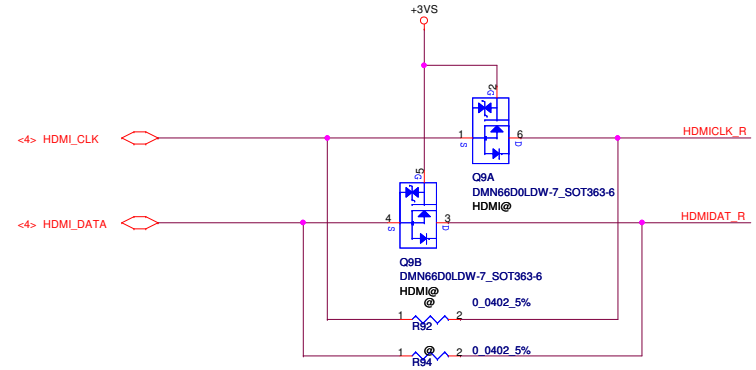






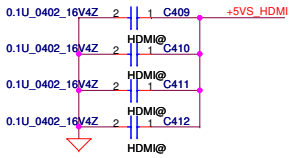


8/26 Change Q7 to SB000009610 Standard Part

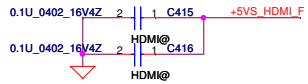


8/19 Change Q9A Q9B to SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6)

10/29 Add C409~C412(0.1U) on +5VS_HDMI



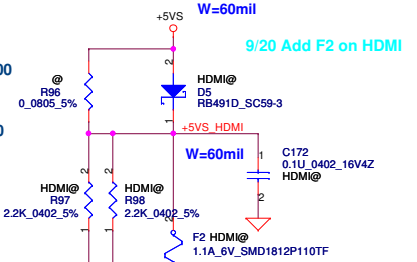
10/29 Add C415~C416(0.1U) on +5VS_HDMI_F



10/27 Change D5 P/N from SC1B491D000 to SCS00003H00

W=60mil

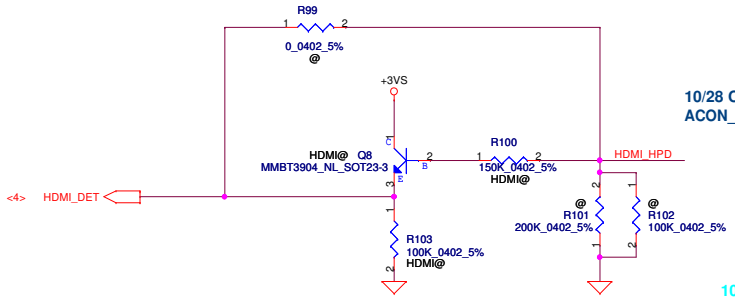
9/20 Add F2 on HDMI



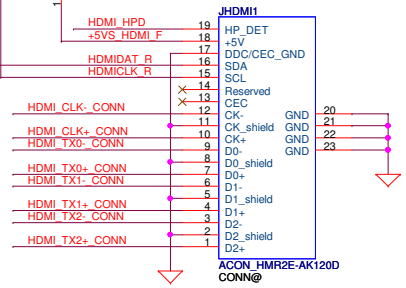
10/27 Change F2 P/N from SP04301P120 to SP040001B00

9/20 Change R99 from HDMI@ to @

9/20 Change Q8,R100 from @ to HDMI@



10/28 Change JHDMI1 footprint from ACON_HMR2E-AK120D_19P-T to ACON_HMR2E-AK120D_19P-S



10/07 Update JHDMI1 footprint from ACON_HMR2E-AK120D_19P to ACON_HMR2E-AK120D_19P-T

8/23 Update JHDMI1 Symbol (SUYIN_100042GR019S268ZR_19P-T)

8/23 Update JHDMI1 Symbol (SUYIN_100042GR019M23DZL_19P-T)

9/7 Update JHDMI1 Symbol (ACON_HMR2E-AK120D_19P)

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.	
Title	HDMI Connector
Size: Custom	Document Number: P0VE6 Schematics
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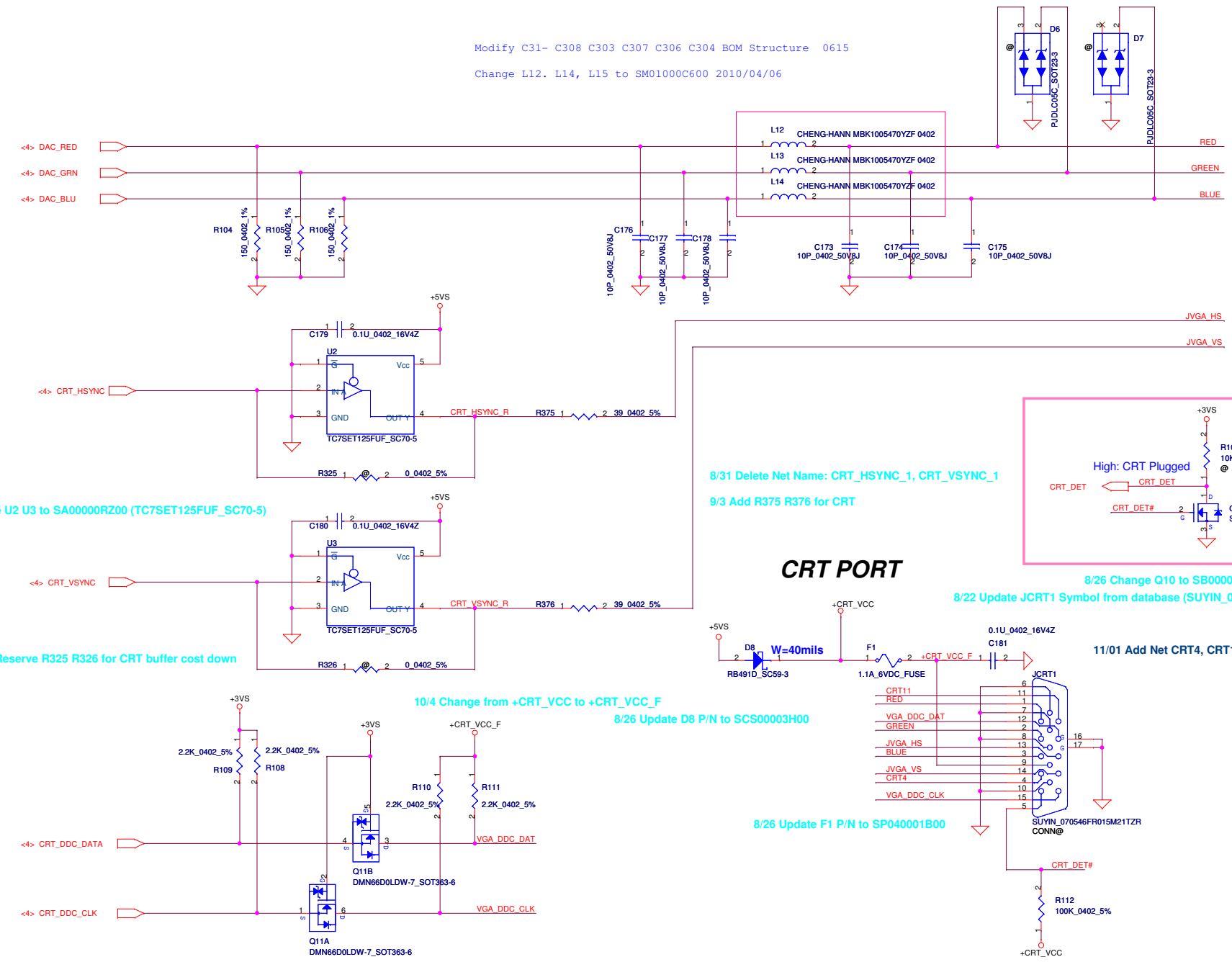
Date: Wednesday, November 17, 2010	Sheet 9 of 36

Close to CRT CONN for ESD.

Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

Change L12. L14, L15 to SM01000C600 2010/04/06



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CRT PORT

Size: B | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 10 of 36

9/9 Add R384(@ 0 ohm) R385(0 ohm) on PCI-E RST

9/20 C183.2 link to R119.2 Follow CRB

10/08 Update U5 to SA000046H70 S IC 218-0792006 A13 HUDSON-M1 605P ABO!

Watchdog timer on NB_PWRGD enable for pull-up disable for pull-down 20100527

9/2 Change R120 from 0603 to 0402

9/16 Change U4,C182 from @ to mount, R120, R115 from mount to @

9/27 Change R115 from @ to mount

9/9 Change R117 R122 from mount to @

9/15 PU PE_GPIO1 100k to +5VALW

10/11 Change Y1 from SJ100006600 to SJ132P7KW10

Close to FCH

9/6 Change PCI-E from FCH to APU

9/15 Change PCI-E from APU to FCH

8/25 Update JBATT1 Symbol (LOTES_AAA-BAT-019-K01_2P)

close to FCH within 1"

10/05 PD 10k(R405) on CLKRUN

8/21 Delete R130,R131(No VGA)

8/23 Add R348 R349 for WWAN PCIE

10/04 Add 100p(C396) on H_PWRGD_L

9/6 Change D10 to SC600000B00 Standard Part

9/13 Add NONCHARGE@ for D10 R244

9/1 Add R372 on CLK_48M_CR

9/7 Change R372 to 22 ohm

11/15 Delete net U5_G22

9/13 Add Net Name +RTCBATT1_RR

9/13 Change Net Name +RTCBATT1 to +RTCBATT2

10/07 Change R140 from 560 to 1k ohm

11/01 Add Net U5_G22 on U5.G22

10/07 Change R392 from 1k to 0 ohm

10/08 Change R392 from 0 ohm to 1k ohm

11/01 Change R392 from 1k to 0 ohm

9/13 Add C392,R392,D23(CHARGE@) for RTC Charge Circuit

SA000046HA0

8/25 Change FCH(U5) PN to SA000046H30

11/04 Change U5 PN to SA000046HA0 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 0FA)

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: FCH PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 11 of 36

8/21 Delete Net : KILL_SW#

9/20 Change R145,R147 from @ to mount

8/31 Pull up 10k(R359) to +3VS on WWAN_CLKREQ#

11/15 Add C417(150p) on H_THERMTRIP#

8/31 Delete Net : SATA_DET#

8/22 Delete Net : R161 R162

10/04 Add 100p(C397) on FCH_PWRGD

9/6 Change ODD_DA#_FCH to USB_OC4#

9/6 Change ODD_DETECT# to USB_OC3#

9/15 Update USB Port List

9/1 Update USB Port List

8/23 USB port8 link to SIM

8/31 Change R182 from mount to @

Change R183 from @ to mount

9/15 Change R178 from @ to mount

10/07 Add R406~R410 (GPIO189~190) for Board ID

10/07 Add E6@(R406) & S6@(R407) for Board ID

10/27 Change R408 R410 from @ to mount

10/28 Add R413 R414 on GPIO192 for project ID

11/15 Change R408,R410,R413 P/N from 10k to 1k SD028100280 to SD028100180

Pull-down for enable high performance mode
20100527 (required for M1)

Internal Pull-Up available

R406	R407	Board ID
mount	@	P0VE6
@	mount	P0VS6

EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM *

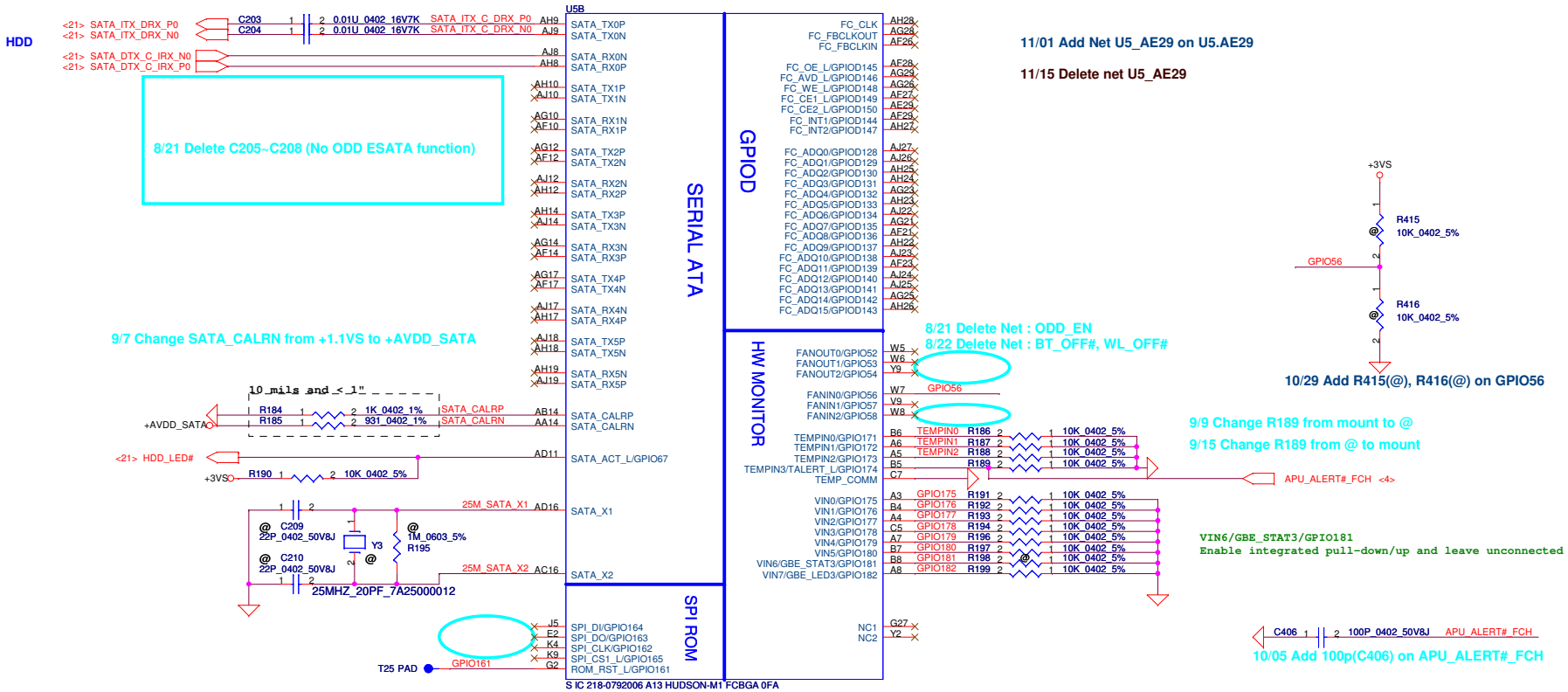
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: FCH HDA/USB/ACPI

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Thursday, November 18, 2010 | Sheet 12 of 36



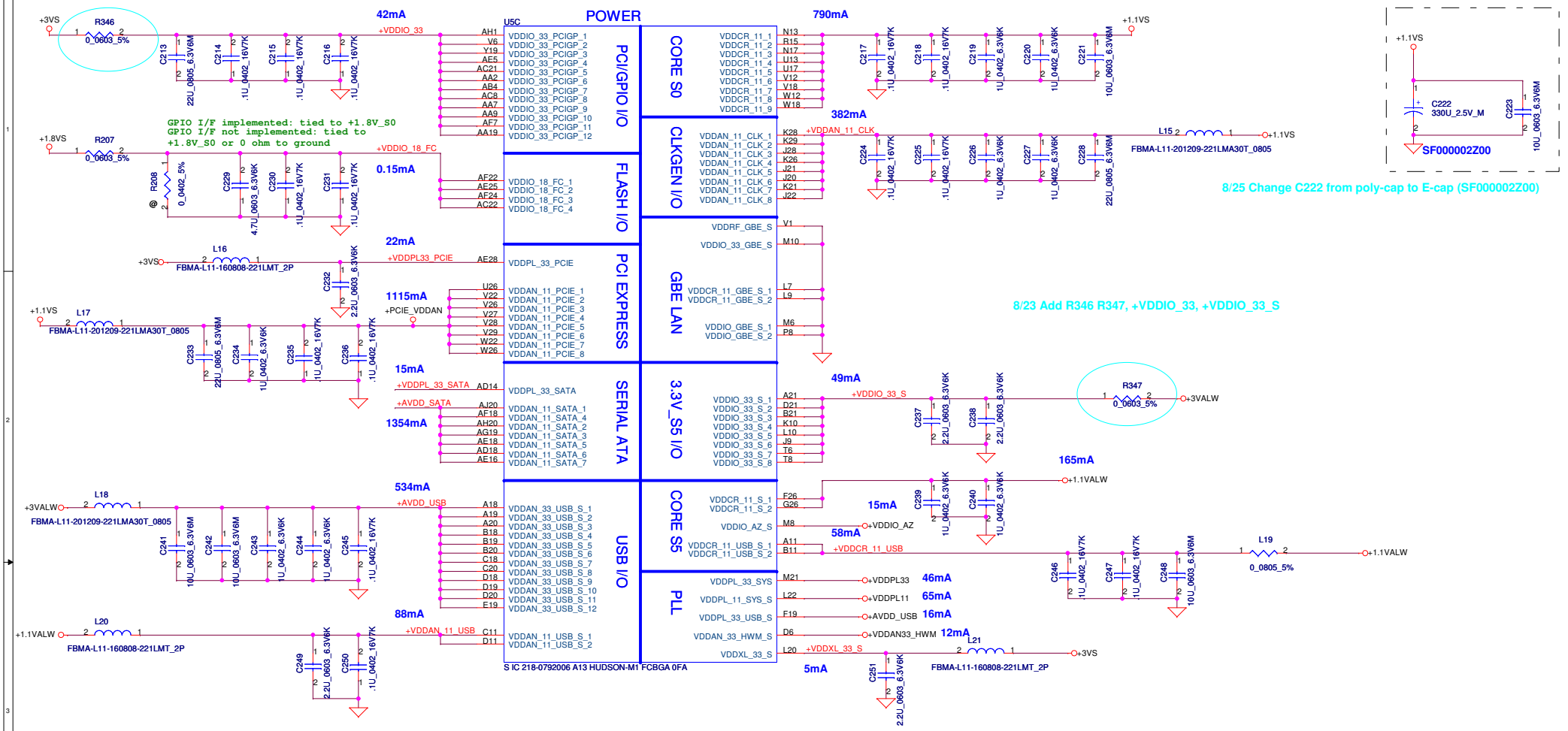
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: FCH-SATA/SPI

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 13 of 36



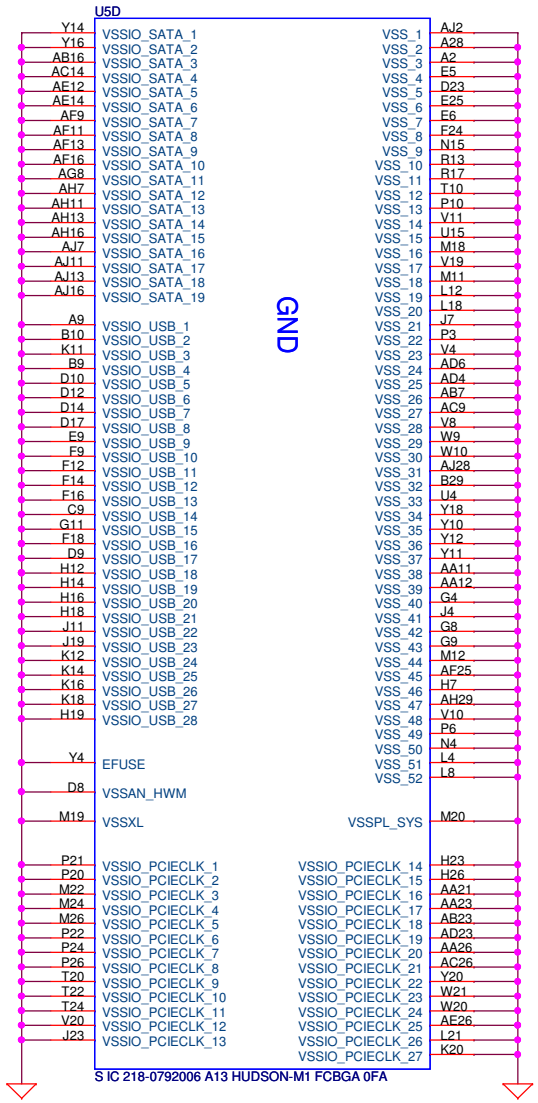
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

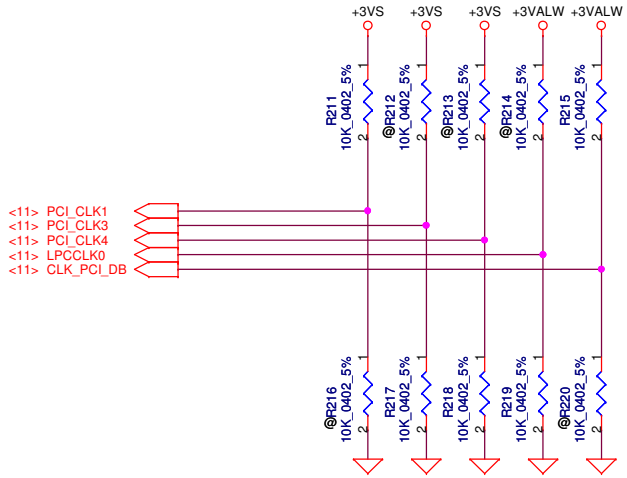
Date: Wednesday, November 17, 2010 | Sheet 14 of 36



REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 *	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode *				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP *	CLKGEN Mode Internal *	internal EC DISABLE *	External CLKGEN Mode				



9/13 Change R211 from mount to @, R216 from @ to mount

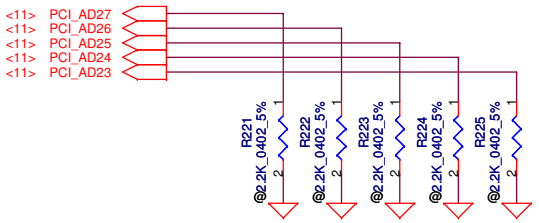
9/13 Change R211 from @ to mount, R216 from mount to @

DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK *	ILA AUTORUN Disabled *	Selects FC PLL *	Disable I2C ROM *	Required Setting *
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size: B | Document Number: P0VE6 Schematics | Rev: 1.0

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Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

08/19 Follow NTUC0
11/04 Change RA19 RA20 from 47k to 10k
08/21 Follow PAV70

Int. Speaker Conn.

20mil
10/26 Remove DA4 CA46 CA47 RA23 RA24
10/28 Add JSPK1 (2 pin)
10/28 Add DA4 CA46 CA47 RA23 RA24
08/25 Change CA5,CA8,CA11,CA13,CA17,CA18,CA19,CA23,CA25,CA26 to SE000004880 Standard Part

40 mil
9/25 Add RA54~RA56
60 mil
20 mil
9/3 Change CA38~ CA43 from 4.7U to 2.2U
Change RA16 from 1k to 100 ohm
9/3 Change RA17 from 1k to 0 ohm
10/11 Change RA40 to 0 ohm (1206)
10/12 Change RA40 to 0.1 ohm (1206)
10/26 Remove SPKR+ SPKR- function
11/17 Change CA40,CA41,RA16 from mount to @
9/6 Update QA2 symbol
Combo Jack
11/17 Change RA11, RA9, CA4, QA1 from mount to @
9/1 Add CA49 RA41 on HP_SENSE
10/28 Reserve CA57 CA58 for EMI
08/31 Reserve CA48(22P) on HDA_SDOUT_AUDIO
11/01 Change CA57, CA58 from @ to mount
Layout Note: close to UA1
9/13 Add RA50~RA53 for DMIC
10/01 Remove RA50,R52
9/6 UA1 Pin 1 link to GNDA
9/7 Change UA1 Pin1 to GND
9/13 Add RA49 for DMIC
11/17 Change RA33 from mount to @
9/7 Add 0.1U (CA50) between GND & GNDA
9/13 Remove Analog MIC circuit
11/17 Change RA12,RA14,CA25 from mount to @
Combo Jack

SA000034010
08/25 Add UA1 PN:SA000034010
10/11 Update UA1 PN:SA000034010
10/12 Update UA1 PN:SA000034010
08/25 Change CA1,CA2,CA3,CA4 to SE000000K80 Standard Part

GND GNDA

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: Audio Codec CX20584

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

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8/23 Reserve 4.7k(RL15) to +3V_LAN on PLT_RST#
Reserve 4.7k(RL16) to +3V_LAN on LAN_CLKREQ#_R

RL15 4.7K 0402 5% LAN_CLKREQ#_R
RL16 4.7K 0402 5% PLT_RST#

UL1 AR8152-AL1E

<11> PCIE_FRX_DTX_P2 — CL6 .1U_0402_16V7K — PCIE_C_RXP1 — TX_P
<11> PCIE_FRX_DTX_N2 — CL9 .1U_0402_16V7K — PCIE_C_RXN1 — TX_N
<11> PCIE_FTX_C_DRX_P2 — RX_P
<11> PCIE_FTX_C_DRX_N2 — RX_N
<11> CLK_PCIE_LAN — CLK_PCIE_LAN — REFCLK_P
<11> CLK_PCIE_LAN# — CLK_PCIE_LAN# — REFCLK_N
<12> LAN_CLKREQ# — RL12 0_0402_5% — LAN_CLKREQ#_R — CLKREQ#
<11,19,20,25> PLT_RST# — PLT_RST# — PERST#
<25> LAN_WAKE# — LAN_WAKE# — WAKE#
<12,19,20> FCH_PCIE_WAKE# — RL14 0_0402_5% — SMCLK — SMDATA
TEST_RST — TESTMODE — GND
LAN_X1 — LAN_X2 — XTLO — XTLI
NC

LED_ACT# — LAN_ACTIVITY#
LED_LINK10_100# — LAN_SK_LAN_LINK#
TRXP0 LAN_MDI0+ RL1 49.9 0402 1%
TRXN0 LAN_MDI0- RL2 49.9 0402 1%
TRXP1 LAN_MDI1+ RL3 49.9 0402 1%
TRXN1 LAN_MDI1- RL4 49.9 0402 1%
close to Lan chip
CL3 0.1U_0402_16V4Z
CL4 0.1U_0402_16V4Z
RBIAS — RL5 2.37K_0402_1% — RL5 keep away other singal (25mil)
W=40mils
VDD33 — +3V_LAN
LX — +LX — W=40mils
W=40mils
VDDCT VDDCT_REG — +VDDCT_REG — +VDDCT
DVDDL DVDDL_REG — +DVDDL — W=40mils
AVDDH AVDDH_REG — +AVDDH — W=40mils
AVDDL AVDDL AVDDL_REG — +AVDDL — W=40mils

2010.08.21 Follow PAWGC
9/9 Change RL14 from @ to mount
Change YL1 to SJ100003300 2010/04/06
YL1 25MHZ_20PF_7A25000012
CL10 27P_0402_50V8J
CL11 27P_0402_50V8J
DL8 @ RB751V-40_SOD323-2
10/11 Change DL8 to SCS00000Z00
9/23 Reserve DL8 on LAN_CLKREQ#

AR8152L PN:SA00003JW30
8/25 Change UL1 P/N to SA00003JW30

* If SWR mode applied,
Mount LL1, CL30, CL14, CL2, CL13 and CL27. No mount RL11 and CL26.
Place LL1 close to LAN Pin40.
* If LDO mode applied,
Mount CL30, CL2, RL11, CL26 and CL27. No mount LL1, CL14 and CL13.

+LX — SWR@ LL1 4.7UH_1008HC-472EJFS-A_5%_1008 — +VDDCT
CL30 0.1U_0402_16V4Z
CL14 SWR@ 1000P_0402_50V7K
CL2 10U_0603_6.3V6M
CL13 SWR@ 0.1U_0402_16V4Z
close to Lan pin5
close to Lan pin40
LDO@ RL11 0_0603_5%
+VDDCT_REG
CL26 LDO@ 1U_0402_6.3V6K
CL27 0.1U_0402_16V4Z
close to Lan pin4

LAN Power circuit refer to NAU00
W=40mils
+3VALW — RL13 0_0603_5% — +3V_LAN
1A
QL1 AP2301GN-HF_SOT23-3
CL5 1000P_0402_50V7K
CL8 0.1U_0402_16V4Z
CL7 1U_0402_6.3V6K
CL1 10U_0603_6.3V6M
CL34 10U_0603_6.3V6M
close to LAN Pin 1
RL18 10K 0402 5% — EN_WOL# <25>
CL41 0.1U_0402_16V4Z
9/2 Reserve Q36, R374, C387 for EN_WOL#
9/2 Change R374 to RL18, C387 to CL41 Q36 to QL1

Change CL17, CL21, CL24, CL26 to SE000000K80 2010/04/06
+AVDDL
close to Lan pin6
close to Lan pin31
CL24 1U_0402_6.3V6K
CL12 0.1U_0402_16V4Z
CL20 0.1U_0402_16V4Z
CL16 0.1U_0402_16V4Z
close to Lan pin34
+AVDDH
CL21 1U_0402_6.3V6K
CL22 0.1U_0402_16V4Z
CL23 0.1U_0402_16V4Z
close to Lan pin9
close to Lan pin22
+DVDDL
CL17 1U_0402_6.3V6K
CL18 0.1U_0402_16V4Z
CL19 0.1U_0402_16V4Z
close to Lan pin37
close to Lan pin24

9/21 Change QL1 from SB934130000 to SB934130020
9/25 Change QL1 to SB000007H10
8/26 Change TL1 P/N to SP050003N00

+VDDCT — LL2 MURATA_BLM18AG601SN1D_0603 — +VDDCT_L
close to LL2
CL25 1U_0402_6.3V6K
CL35 1000P_0402_50V7K
CL31 0.1U_0402_16V4Z
CL36 1000P_0402_50V7K
CL29 0.1U_0402_16V4Z
close to TL1

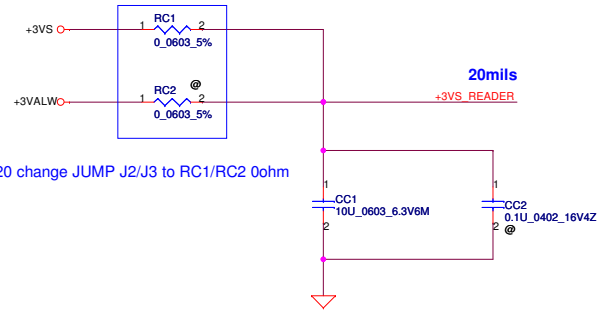
TL1 350uH_NS0013LF
LAN_MDI1+ LAN_MDI1- LAN_MDI0+ LAN_MDI0-
RD+ RD- CT NC NC CT TD+ TD-
RX+ RX- CT NC NC CT TX+ TX-
RJ45_MDI1+ RJ45_MDI1- RJ45_CT0 RJ45_CT1 RJ45_MDI0+ RJ45_MDI0-
RL7 75_0402_5%
RL6 75_0402_5%
CL15 1000P_1206_2KV7K — RJ45_GND
SP050003N00
9/2 Reserve DL2~7 for EMI(Need Update)
9/7 Update DL2~DL5 symbol from database
DL2 DL3 DL4 DL5 SMF10A_SOD-123FL2
DL6 DL7 B88069X9231T203_4P5X3P2-2
9/9 Update DL6~DL7 symbol from database

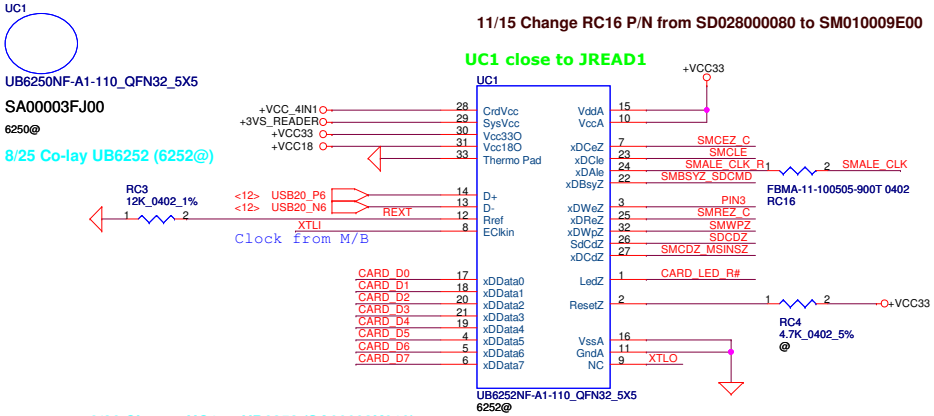
close to JRJ45
CL28 470P_0402_50V7K
LAN_ACTIVITY# — RL9 511_0402_1% — LAN_ACTIVITY#_R
RL10 5.1K_0402_5%
JRJ45 SANTA_130452-3 CONN@
Yellow LED+ Yellow LED- Green LED+ Green LED-
SHLD1 SHLD1
PR4- PR4+ PR2- PR3- PR3+ PR2+ PR1- PR1+
DETECT PIN1
RJ45_MIDI1- RJ45_MIDI1+ RJ45_MIDI0- RJ45_MIDI0+
For EMI.
CL32 470P_0402_50V7K
+3V_LAN — RL8 511_0402_1% — LAN_SK_LAN_LINK#_1
LAN_SK_LAN_LINK#
CL33 470P_0402_50V7K
CL38 1000P_1206_2KV7K — RJ45_GND
LANGND
CL39 0.1U_0402_16V4Z
CL40 0.1U_0402_16V4Z
LL3 MCK3225201YZF_2P
DL1 PJDLC05C_SOT23-3
9/2 Change R399 to RL17
9/3 Remove RL17
9/2 Reserve R399(0 ohm) on LAN_SK_LAN_LINK#
9/1 Add DL1, CL38~40,LL3 for EMI
9/2 Change RJ45_GND to LANGND on DL1

AR8152	Pin No.	PU/PD	Description
LED[0]	38	L	un-overclocking
		H	overclocking
LED[1]	39	L	LDO mode
		H	SWR mode

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

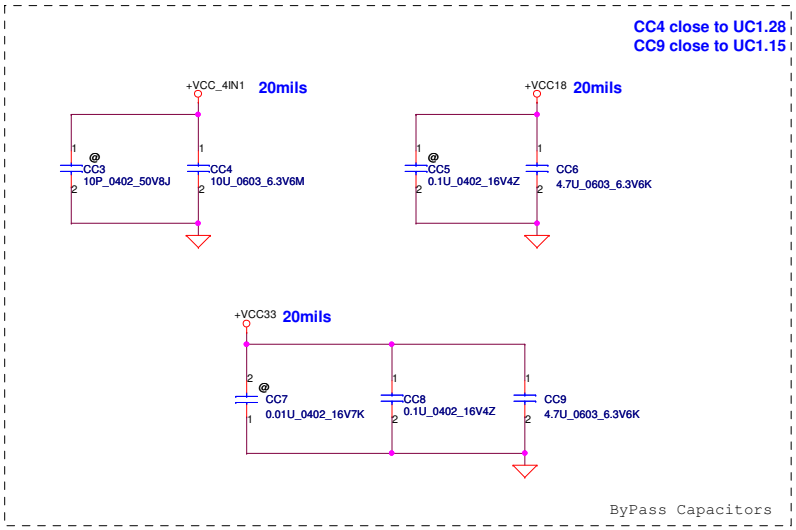
Compal Electronics, Inc.
Title: LAN AR8152
Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0
Date: Wednesday, November 17, 2010 | Sheet 17 of 36



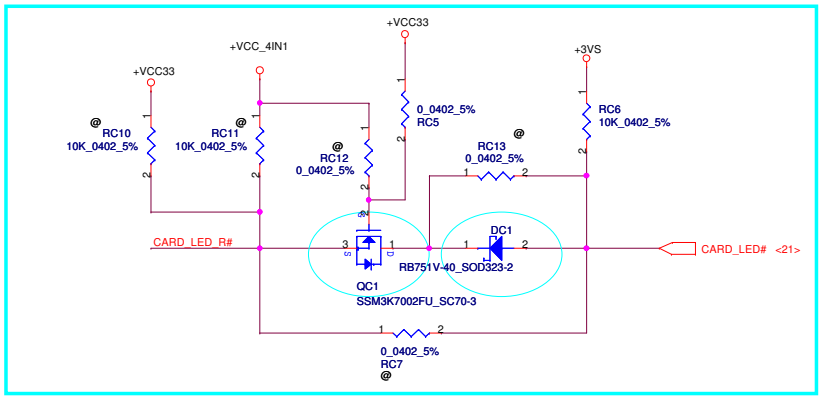


8/26 Change UC1 to UB6252 (SA00003K010)

If use external crystal (YC1), UC1 will change to UB6252

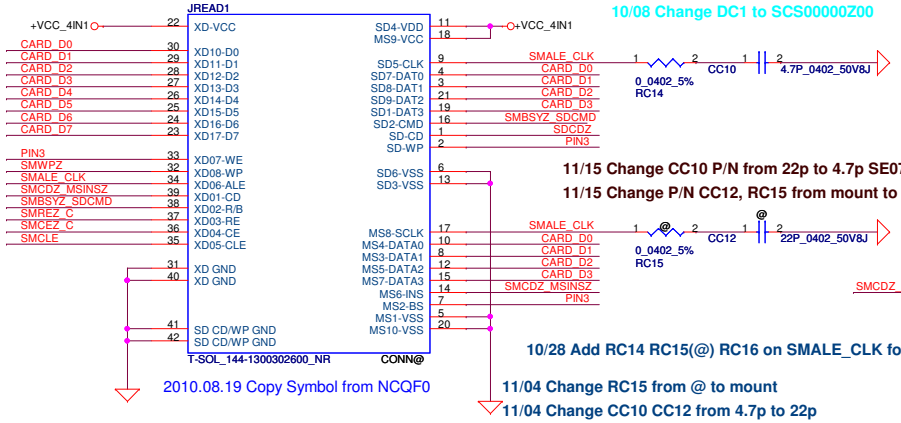


8/24 Card_LED# Follow PAV70

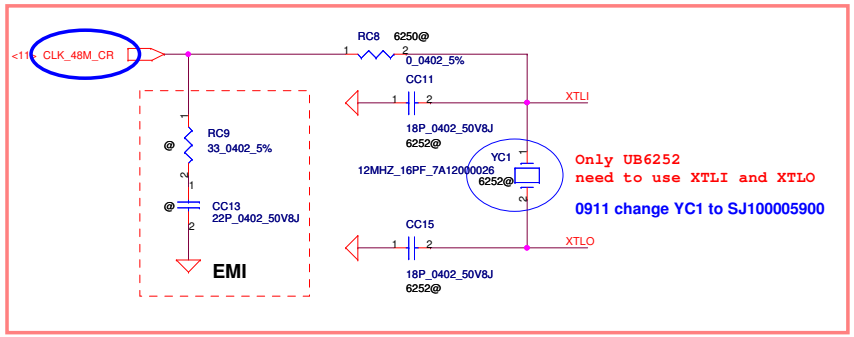


Card Reader Connector

8/26 Change DC1 to SCS00002G00 Standard Part
8/26 Change QC1 to SB000009610 Standard Part
10/08 Change DC1 to SCS00000Z00



11/15 Change CC10 P/N from 22p to 4.7p SE071220J80 to SE07147AC80
11/15 Change P/N CC12, RC15 from mount to @.
10/28 Add RC14 RC15(@) RC16 on SMALE_CLK for EMI
2010.08.19 Copy Symbol from NCQF0
11/04 Change RC15 from @ to mount
11/04 Change CC10 CC12 from 4.7p to 22p



9/2 Change CC11 CC15 from 27P to 18P

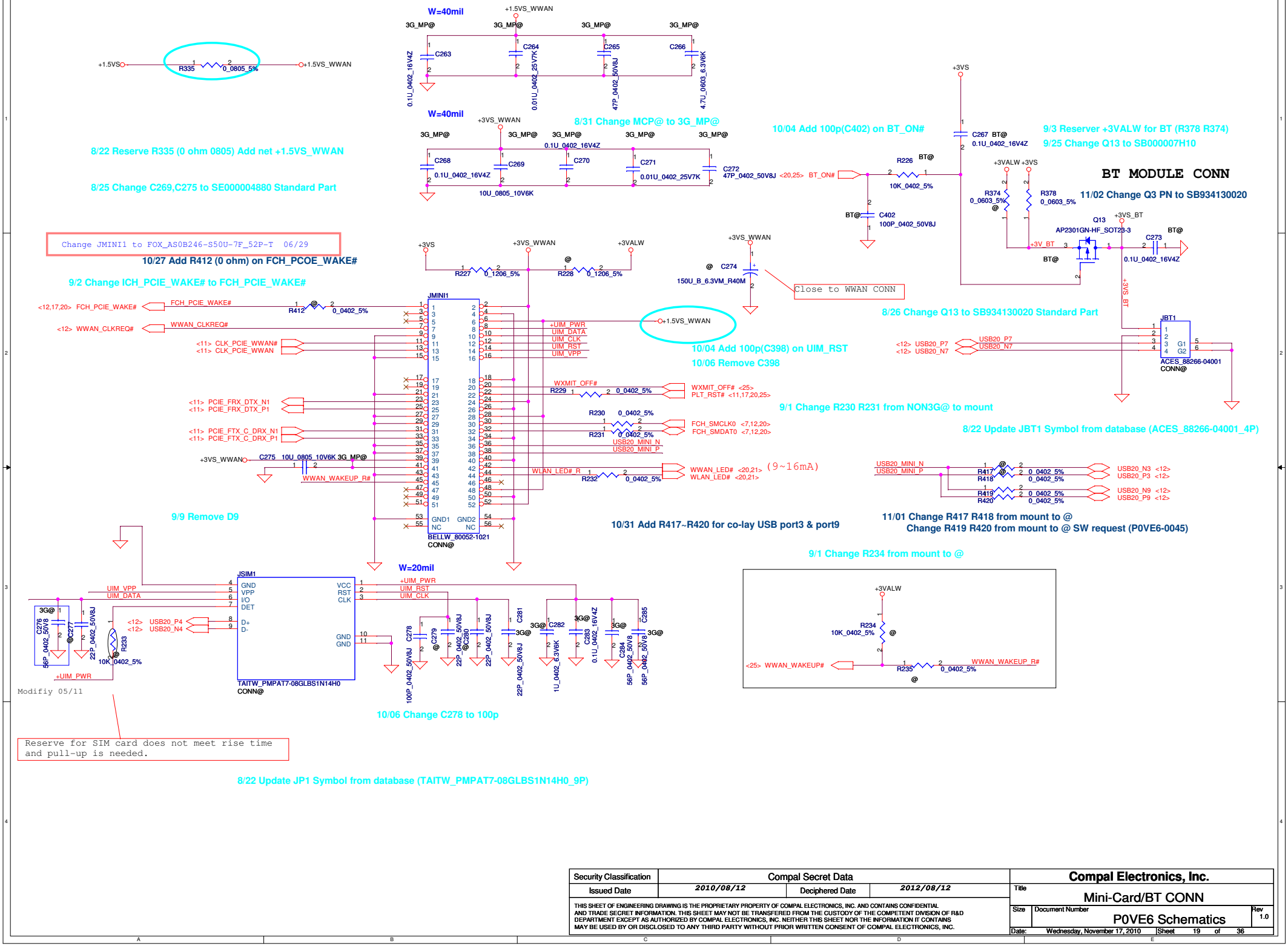
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CARD READER UB6250/6252

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

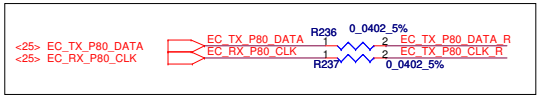
Date: Wednesday, November 17, 2010 | Sheet 18 of 36



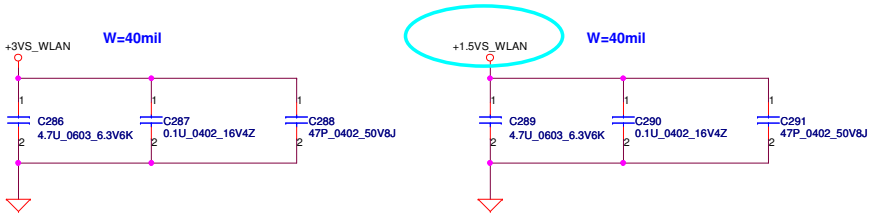
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

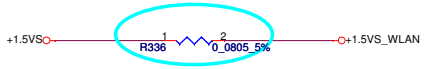
Compal Electronics, Inc.	
Title	Mini-Card/BT CONN
Size	Document Number: P0VE6 Schematics
Rev	1.0
Date: Wednesday, November 17, 2010	Sheet 19 of 36

Mini-Express Card for WWAN



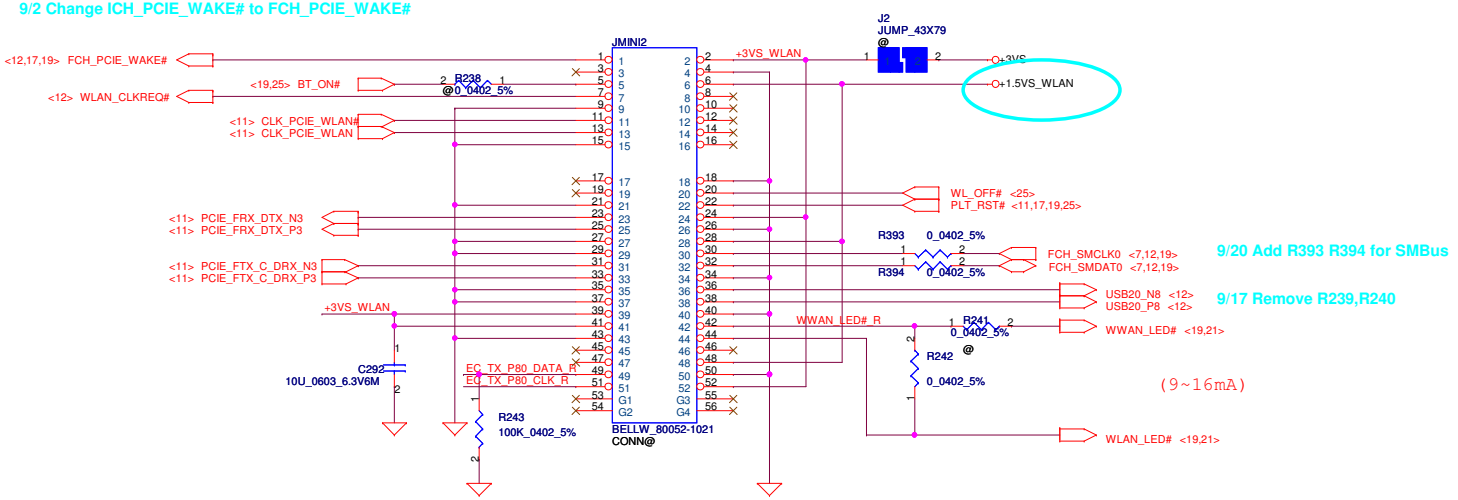
Mini-Express Card for WLAN





8/22 Reserve R336 (0 ohm 0805) Add net +1.5VS_WLAN

9/2 Change ICH_PCIE_WAKE# to FCH_PCIE_WAKE#



9/20 Add R393 R394 for SMBus

9/17 Remove R239,R240

(9~16mA)

5/12 Update WLAN connector(the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

Compal Electronics, Inc.			
Title: WLAN	WLAN		
Size: Custom	Document Number: P0VE6 Schematics	LA-6222P	Rev: 1.0
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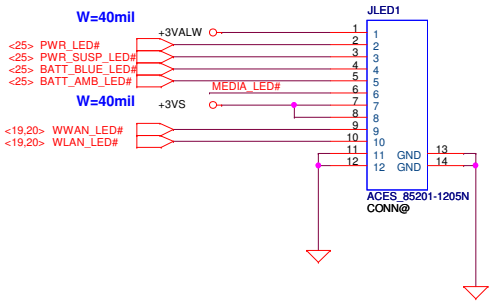
LED PCB CONN

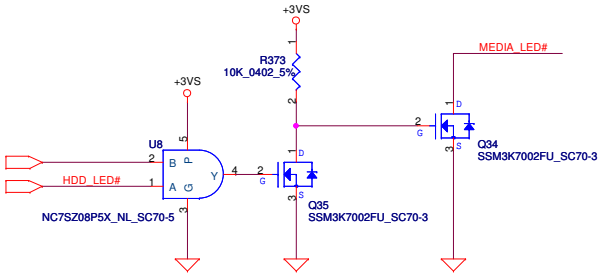


8/22 Update JP2 Symbol from database (ACES_85201-1605N_16P)

8/24 Update JLED1 Symbol from database (ACES_85201-1205N_12P) & Update pin definition

9/1 Add LED Circuit (LED2~4(SC597UDB000)LED5(SC5191NB000), R360~R369, Q33)

9/1 Change All LED power to 5V



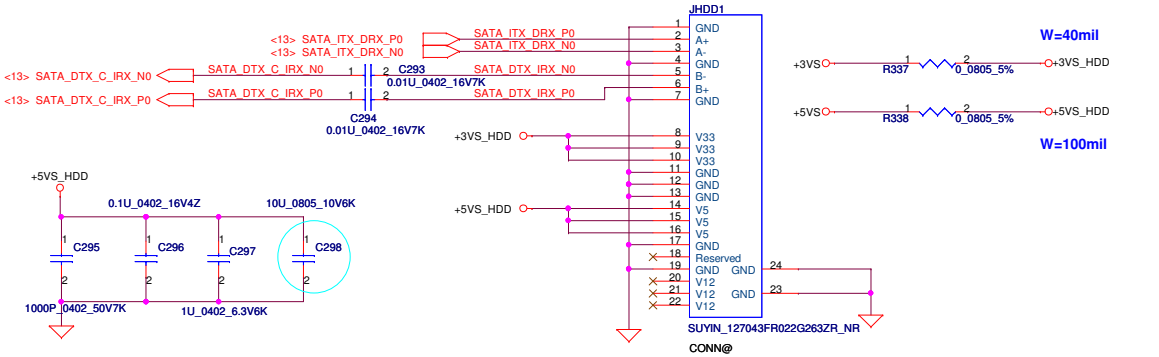
9/1 Add R373, Q34, Q35 for MEDIA_LED#

9/9 Change LED2~4 footprint to LED_HT-297DQ-GQ_4P

9/11 Remove LED portion

SATA HDD Conn.

8/22 Reserve R337 R338 Add net +3VS_HDD,+5VS_HDD



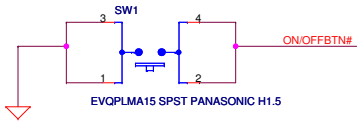
9/1 Change Q33 to SB000009610(SSM3K7002FU_SC70-3)

8/22 Change C298 from 10U 6.3V to 10U 10V

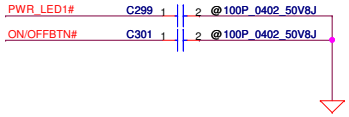
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.			
Title	SATA CONN./LED/B CONN./BATT CONN.		
Size B	Document Number	P0VE6 Schematics	Rev 1.0
Date: Wednesday, November 17, 2010	Sheet 21 of 36		

ON/OFF Button



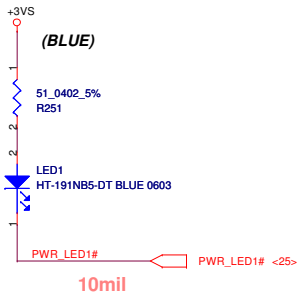
FOR EMI



9/6 Change D13 from mount to @
10/05 Remove D13

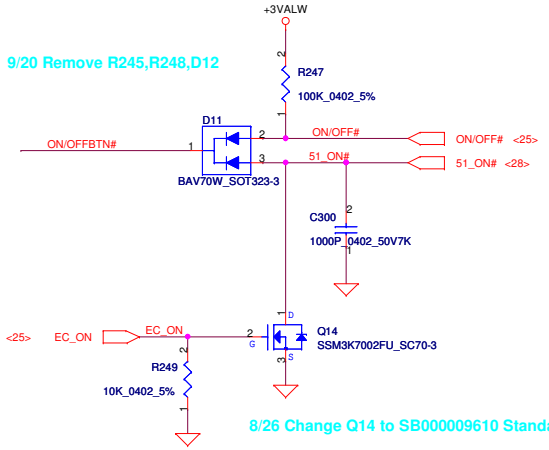
9/1 Remove LED2 LED3 circuit, Change 70@ to mount

9/20 Add LED2 LED3 Circuit
9/21 Remove LED2 LED3 Circuit



8/26 Change D11 to SC600000B00 Standard Part

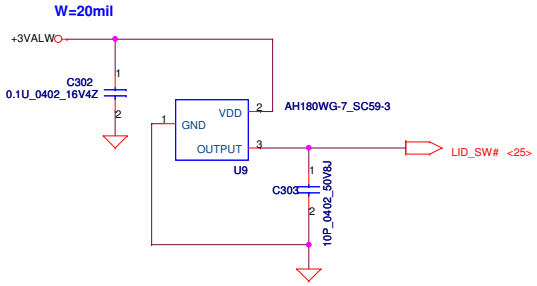
9/20 Remove R245,R248,D12



8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

LID Switch



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: ON/OFF / PWR SW/ LID SW

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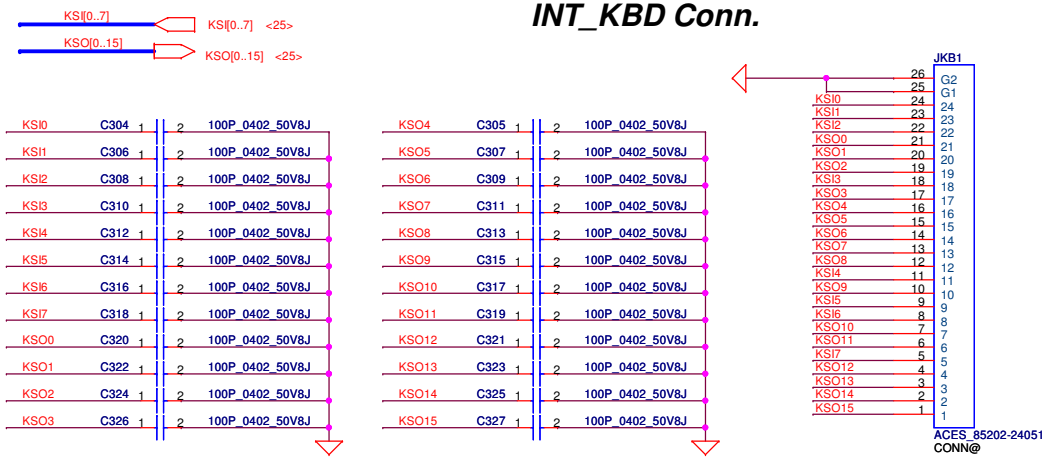
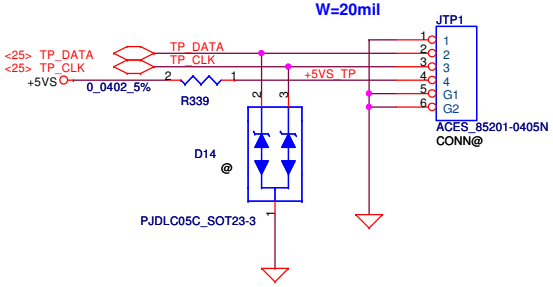
INT_KBD Conn.



8/22 Update JKB1 Symbol from database (ACES_85202-24051_24P)
8/23 Update KB pin definition

To TP/B Conn.

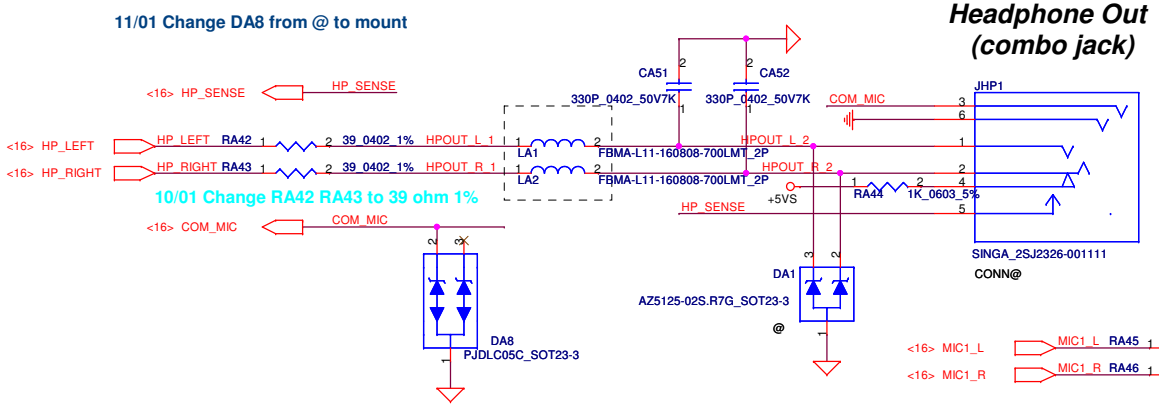
8/22 Update JP3 Symbol from database (ACES_85201-0605N_6P)
8/22 Reserve R339 (0 ohm 0402) Add Net name +5VS_TP



8/24 Update JTP1 Symbol from database (ACES_85201-0405N_4P)
& Update pin definition

Headphone Out (combo jack)

11/01 Change DA8 from @ to mount



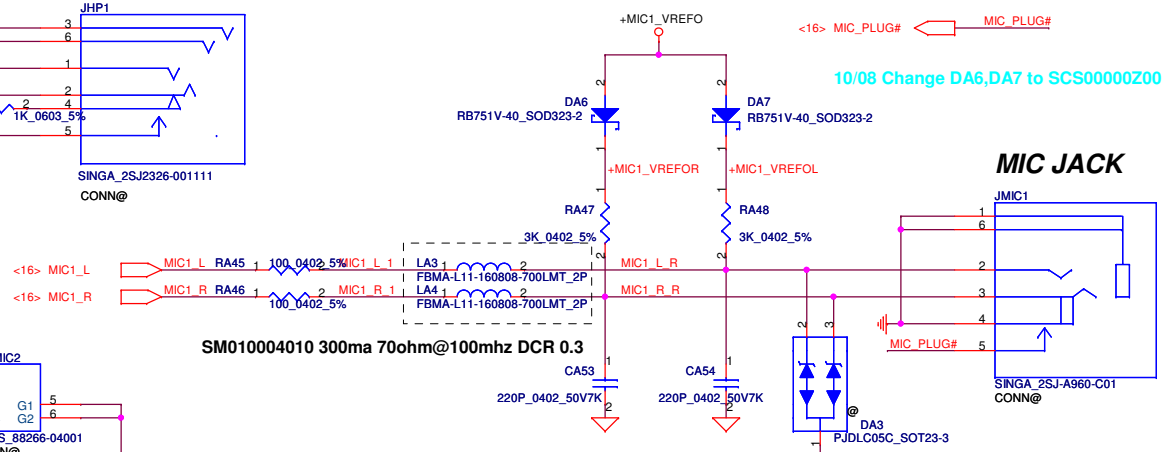
10/06 Change Jacks GND to GNDA

9/28 Change Jacks AGND to GND

9/13 Combine LS-7071PR01_USB_0908.DSN Audio Jack Portion

10/08 Change DA6,DA7 to SCS00000Z00

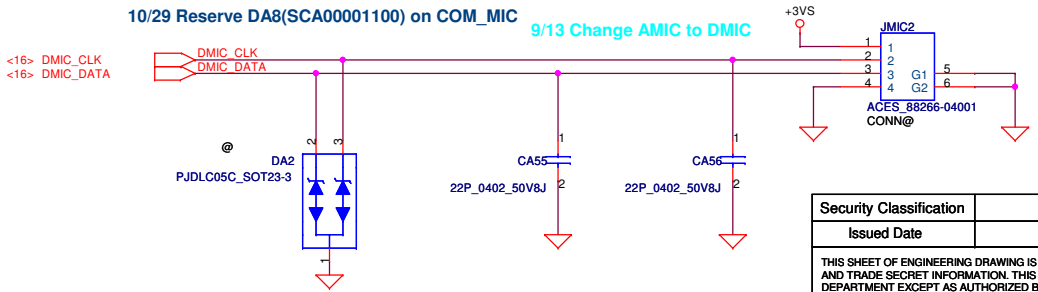
MIC JACK



SM010004010 300ma 70ohm@100mhz DCR 0.3

10/29 Reserve DA8(SCA00001100) on COM_MIC

9/13 Change AMIC to DMIC



9/14 Update JMIC1 to DC230007700(SUYIN_010030HR006G129ZR_6P)
9/17 Update JMIC1 to DC230004K00(SINGA_2SJ-A960-C01_6P)

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: KB Conn/TP/CR Conn

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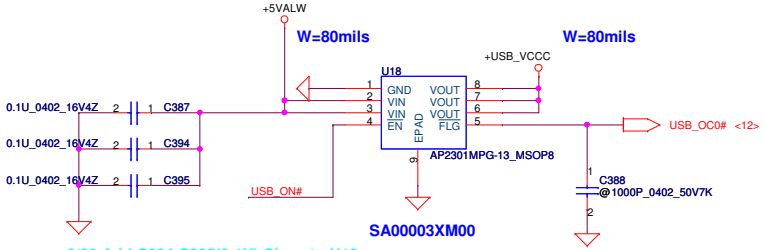
USB Charge Follow PAWGC

8/25 Remove Charge USB Circuit

9/1 Add R370 R371 for OC circuit

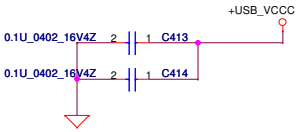
9/15 remove R370 R371 for OC circuit

Left Side USB CONN.



9/29 Add C394,C395(0.1U) Close to U18

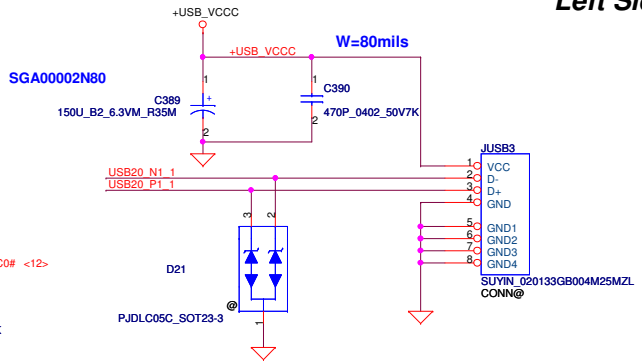
9/11 Combine USB/B circuit

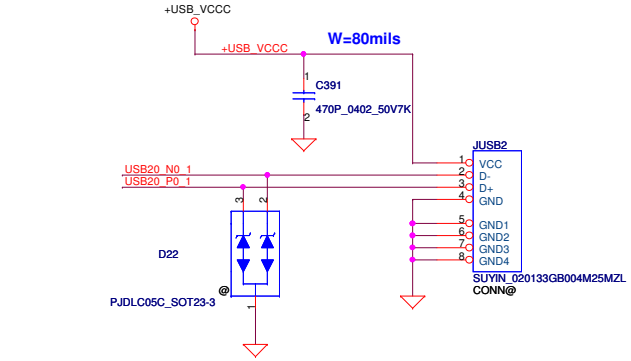


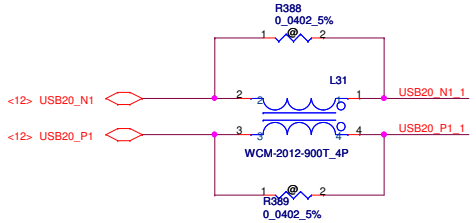
10/29 Add C413~C414(0.1U) on +USB_VCCC

9/11 Change C340 C389 to SGA00002N80

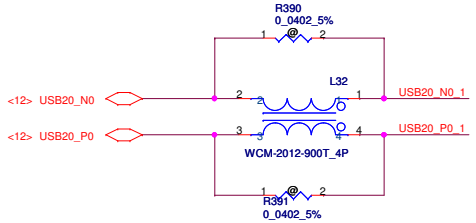
9/24 Change U11,U18 to SA00003XM00







9/28 Swap L31 L32

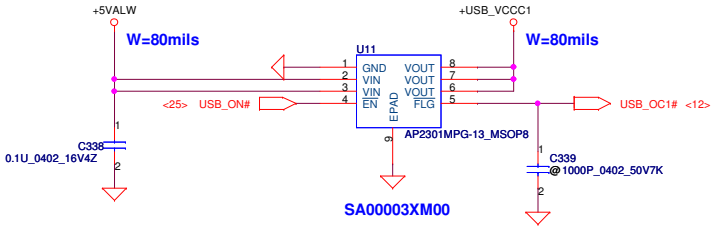


10/28 Change R388,R389,R390,R391,R257,R258 from mount to un-mount

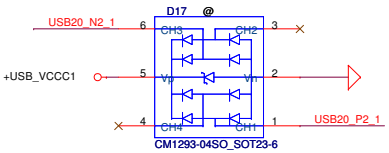
10/28 Change L28,L31,L32 (SM070000K00) from un-mount to mount

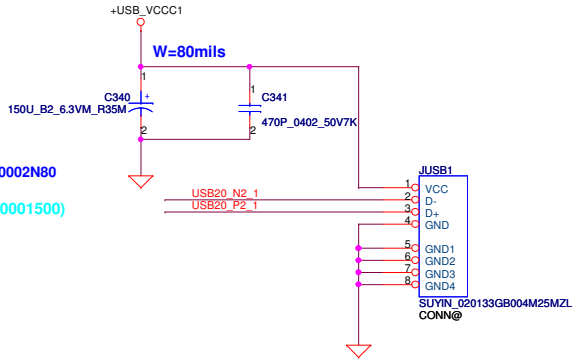
9/27 Change L28,L31,L32 to SM070000K00

Right Side USB CONN.

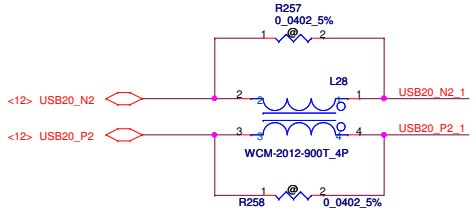


8/25 Change C340 from poly-cap to E-cap (SF000001500)





9/28 Swap L28



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: USB PORTS

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11/15 Change L29,L30 P/N from SM010015410 to SM010004010

8/23 Pull up 10k (R345) to +3VALW on USB_ON#

8/31 Change EC_MUTE# Pull-up to +3VS(@)

8/21 Change R262 from 0 ohm 0805 to 0 ohm 0603

W=40mils

W=20mils

9/23 Update EC pin definition follow P5WE6

10/04 Add 100p(C399) on ACOFF

8/26 Change D18 to SCS00002G00 Standard Part

9/23 Reserve R395 on ACIN

10/08 Change D18 to SCS00000Z00

Follow PAWGC

8/23 Delete DAC_BRIG

8/25 Delete CHG_ON#

8/31 Add EN_FAN1 on U12.70

11/02 Change C353 to 10p R275 to 22 ohm

8/23 Change R271 R279 from mount to @

Reserve for EMI please close to U12

9/5 Change R276 R277 from mount to @

8/31 EC_SCI# Pull up to +3VALW

8/25 Delete KSO16 KSO17

8/23 Delete R280

9/25 Change VLDT_EN to VLDT_EN#

9/17 Change Net Name from BATT_GRN_LED# to BATT_BLUE_LED#

8/23 Delete W_DISABLE#_2

10/04 Add 100p(C400) on VR_ON

10/05 Add 100p(C407) on APU_ALERT#_EC

8/24 Delete Net FAN_SPEED1

10/11 Change C354,C355, X1 from @ to mount

8/23 Change R282 from mount to @

X1 C354 C355 from @ to mount

8/26 Change R282 from @ to mount

X1 C354 C355 from mount to @

8/31 Add 100k(R358) pull-down on SUSCLK

10/11 Change R282 R358 from mount to @

8/22 Add R340~R343 (0 ohm)

8/31 Change EC_FAN_PWM from pin 34 to pin 26

8/31 Change PWR_SUSP_LED from pin 36 to pin 34

8/31 Change EC_PME# from pin 118 to pin 103

10/27 Change C356 from 10V_0805 to 6.3V_0603

9/21 Change Q29 from SB000008J00 to SB000009610

9/9 Change R323 from mount to @

8/21 Change R283 from 100k to 0 ohm

Battery APU

Board ID
Analog Board ID definition,
Please see page 3.

Project ID

PME Follow PAWGC

SA00003QQ10

KB930QF A1 LQFP 128P
20mil

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: EC ENE-KB930

Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

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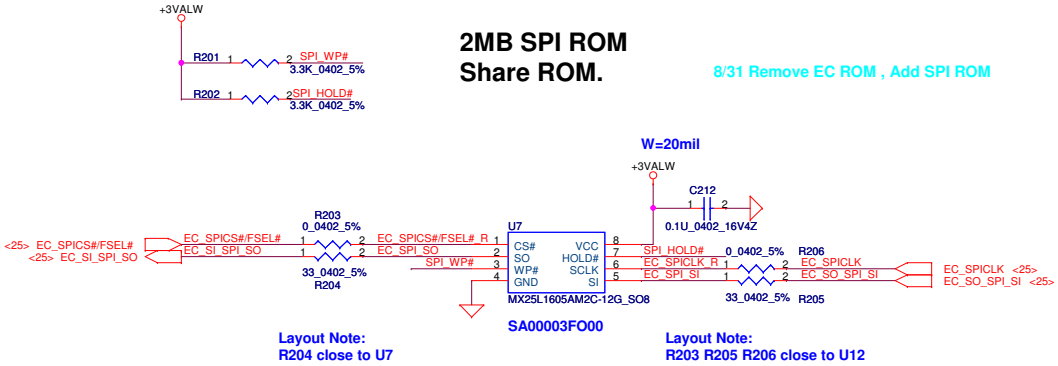
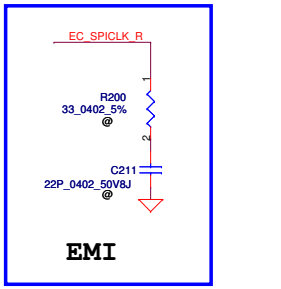
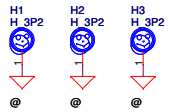


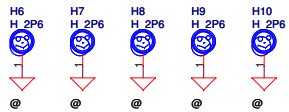


3P2 x 3 (APU)

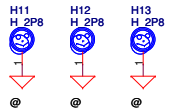


9/15 Update the Screw Hole
9/20 Add H20 (H_3P4X3P2N)

2P6 x 5



2P8 x 3



10/07 Change H13 from GND to LANGND
10/07 Change H13 from LANGND to GND

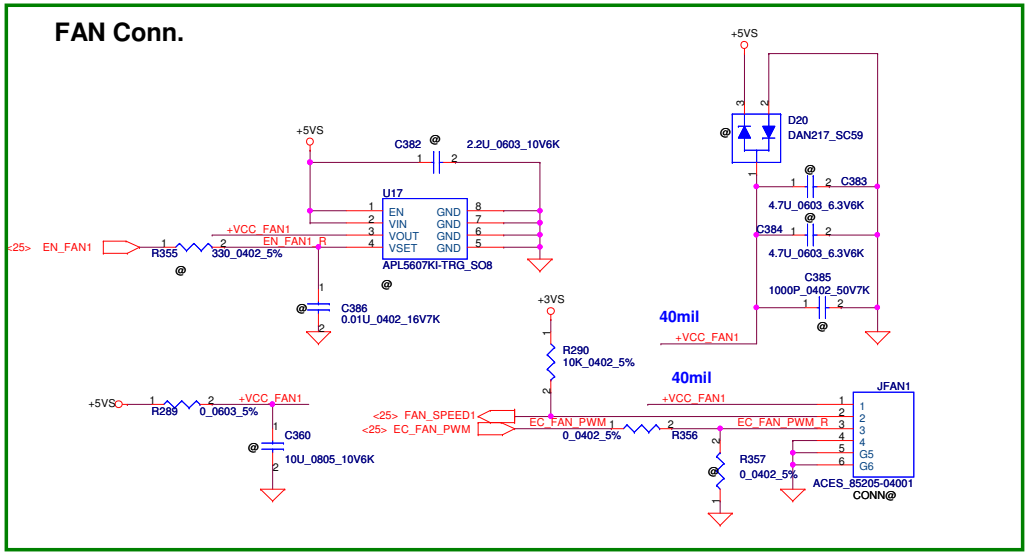
3P2N x 1

H_3P2X3P5N x 1

H_3P2X3P7N x 1

3P3N x 1

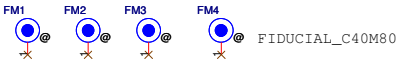
H_3P4X3P2N x 2



8/24 Update JFAN1 Symbol from database (ACES_85205-03001_3P) & Update pin definition
8/24 Delete R290

8/25 Update JFAN1 Symbol from database (ACES_85205-04001_4P) & Update pin definition
8/25 Add R290 10k pull-up tp +3VS

8/31 Reserve U17,C382~C386, R355~R357, D20 (Fan Drive Circuit)



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: Screw / EC ROM /FAN

Size	Document Number	Rev
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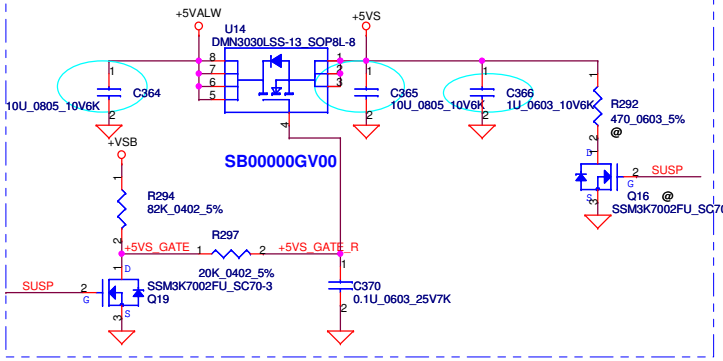
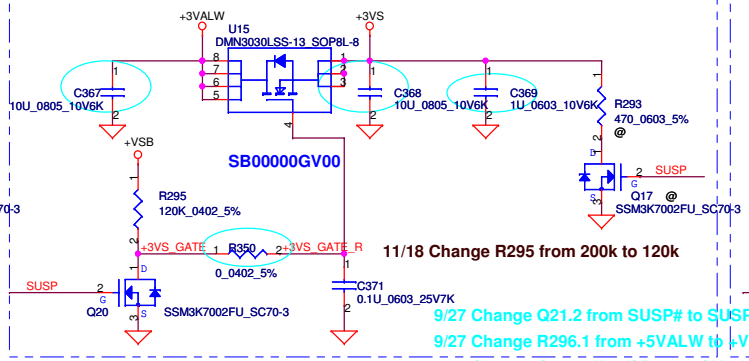
+5VALW TO +5VS



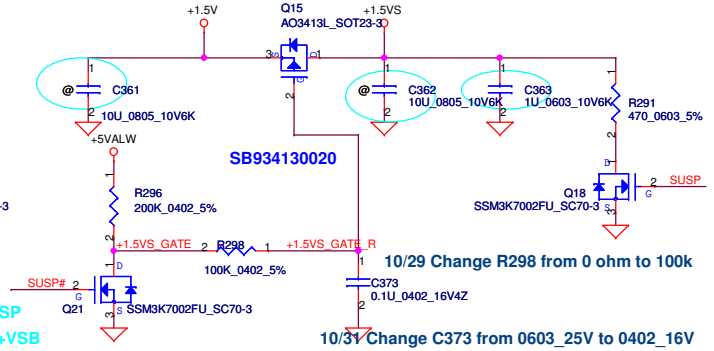
+3VALW TO +3VS



11/18 Change R295 from 200k to 120k

+1.5V to +1.5VS

10/27 Change R291 Q18 from @ to mount



10/29 Change R298 from 0 ohm to 100k

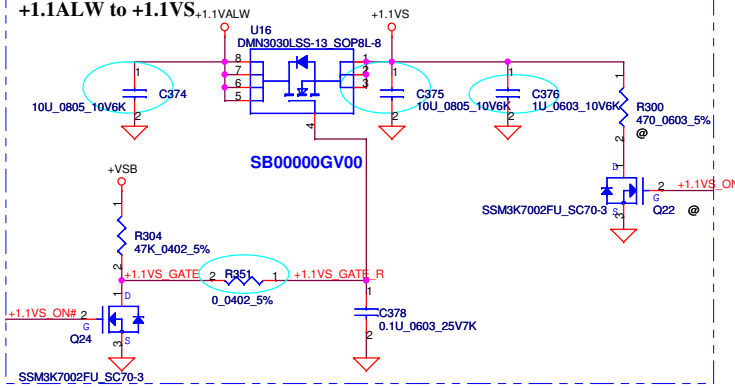
10/31 Change C373 from 0603_25V to 0402_16V

9/27 Change Q21.2 from SUSP# to SUSP

9/27 Change R296.1 from +5VALW to +VSB

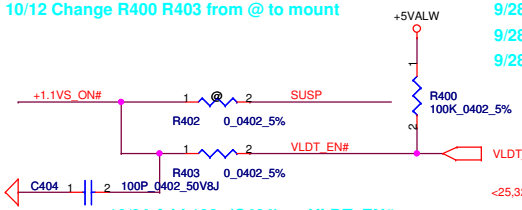
9/27 Change Q15 to U19(SB00000GV00)

+1.1ALW to +1.1VS



10/12 Change R402 from mount to @

10/12 Change R400 R403 from @ to mount



10/04 Add 100p(C404) on VLDT_EN#

10/06 Change C404 on +1.1VS_ON#

9/28 Change Q21.2 from SUSP to SUSP#

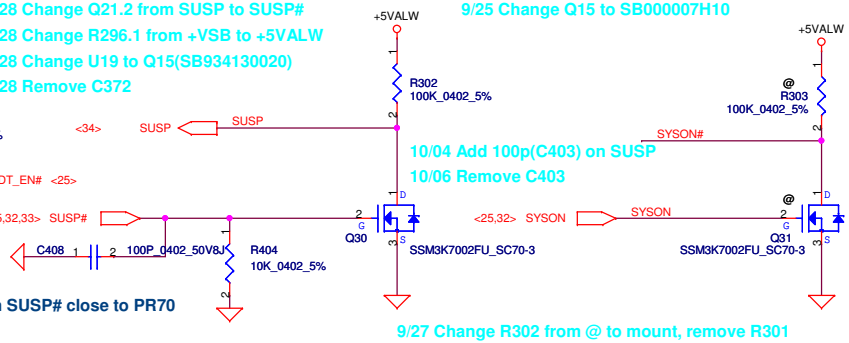
9/28 Change R296.1 from +VSB to +5VALW

9/28 Remove C372

9/28 Change U19 to Q15(SB934130020)

8/26 Change Q15 to SB934130020 Standard Part

9/25 Change Q15 to SB000007H10



10/04 Add 100p(C403) on SUSP

10/06 Remove C403

9/27 Change R302 from @ to mount, remove R301

10/27 Add C408(100P) on SUSP# close to PR70

9/27 Change R304.1 from +5VALW to +VSB

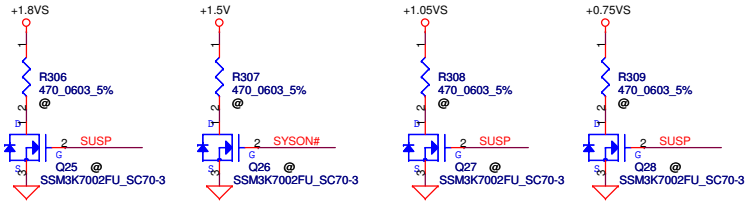
10/12 Change R294 to 100k

10/12 Change R295, R296 to 200k

10/12 Change R304 to 47k

10/12 Change R294 to 82k

10/12 Change R297 to 20k



8/19 Change Q16~Q22 Q24~Q28 toSB000009610(SSM3K7002FU_SC70-3)

8/19 Change Q29 Q30 to Q23A Q23B (SB00000DH00 S TR DMN66D0LDW-7 2N SOT363-6)

8/21 Change U14~U16 to SB548000310 (SI4800BDY-T1-E3_SO8)

8/23 Remove R305 R299 Add R350 R351 for Sequence

8/24 Change Q23A Q23B to Q30 Q31(@) (SB000009610 SSM3K7002FU_SC70-3)

8/25 Change C363,C366,C369,C376 to SE080105K80 Standard Part

8/25 Change C361,C362,C364,C365,C367,C368,C374,C375 to SE000004880 Standard Part

8/26 Change U14, U15, U16 to SB00000GV00 Standard Part

9/3 Delete C377(DIS@)

9/23 Reserve R400~403, Q36 for VLDT_EN

9/25 Remove R401 Q36 on VLDT_EN

9/25 Add 10k(R404) PD on SUSP#

10/31 Change C361 C362 from mount to @

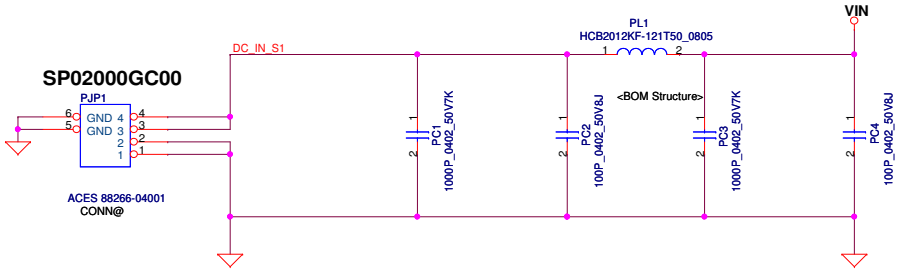
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

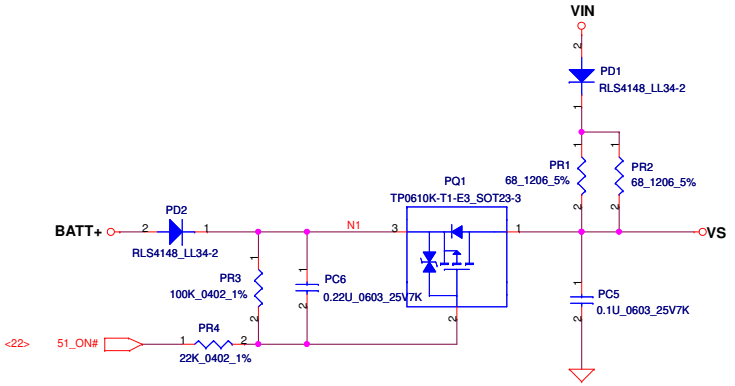
Compal Electronics, Inc.

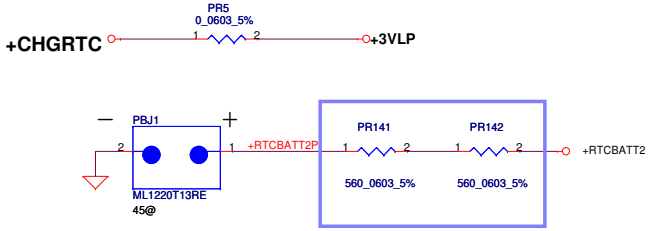
Title: DC Interface

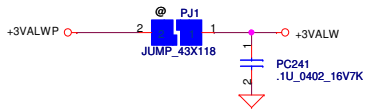
Size: Custom | Document Number: P0VE6 Schematics | Rev: 1.0

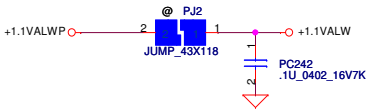
Date: Thursday, November 18, 2010 | Sheet 27 of 36

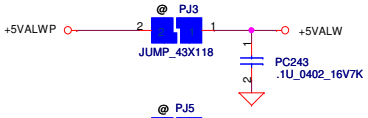


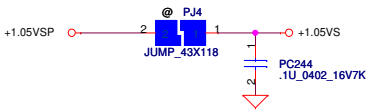


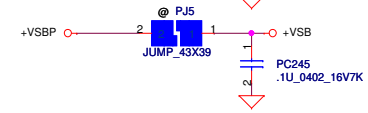


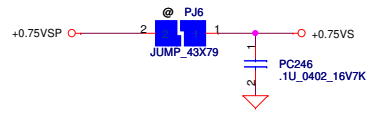


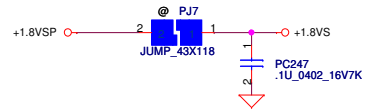


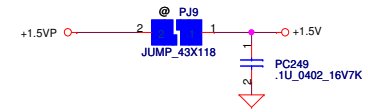












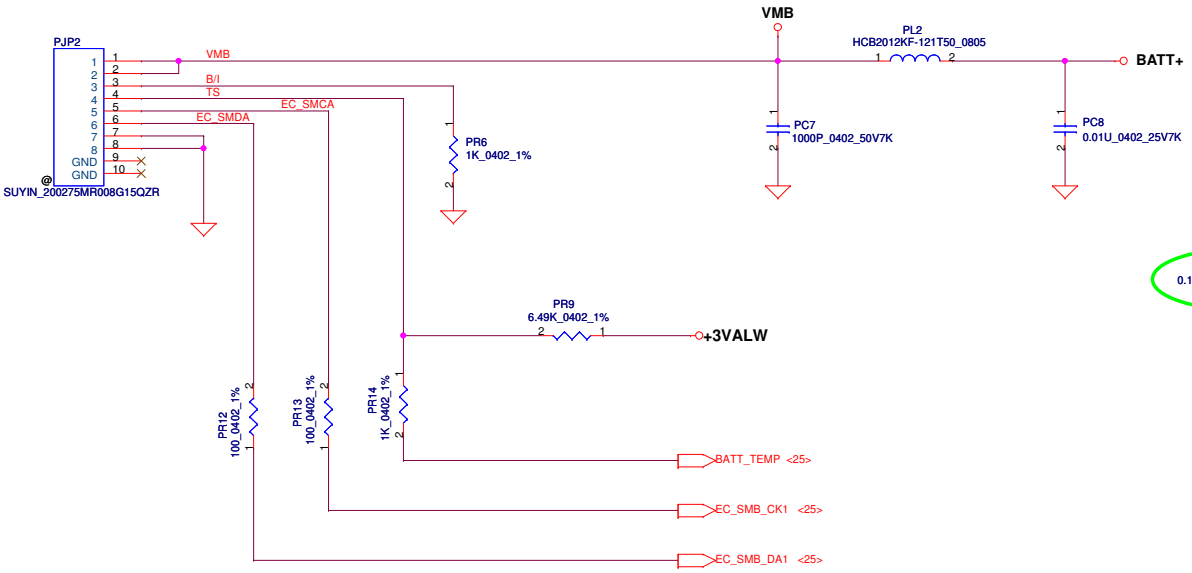
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: DCIN/VIN DECTOR

Size	Document Number	Rev
		1.0

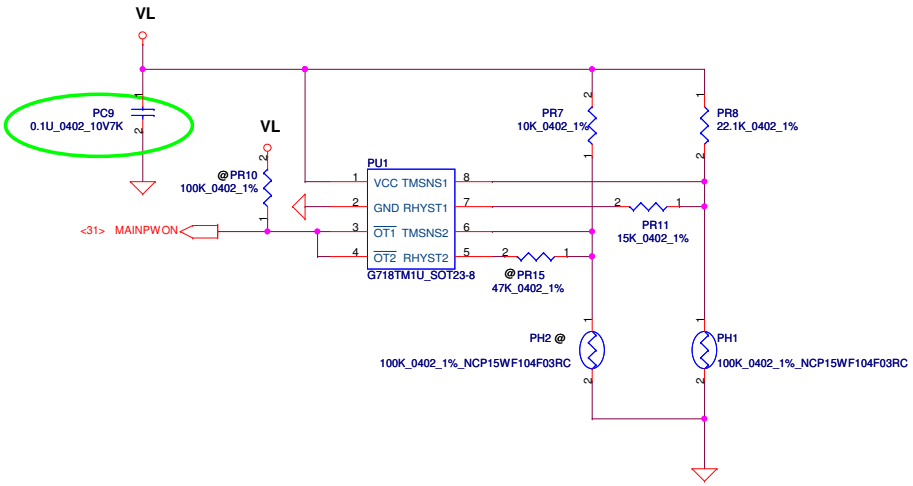
Date: Wednesday, November 17, 2010 | Sheet 28 of 36

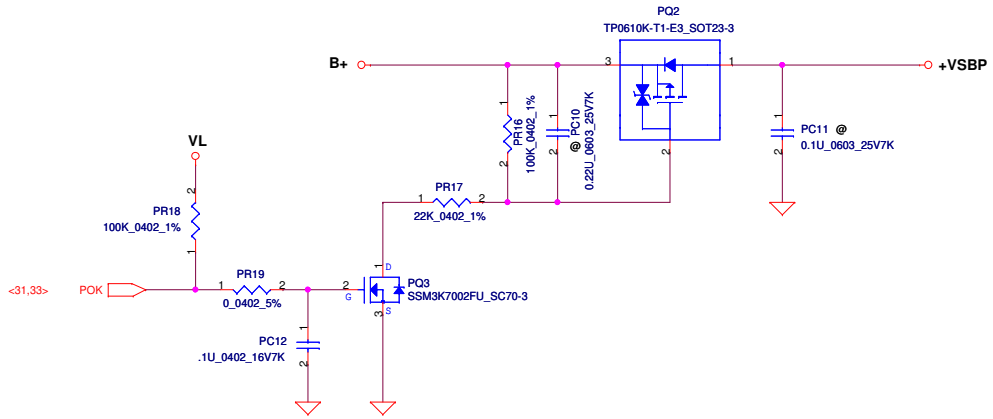


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 72 degree C





Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

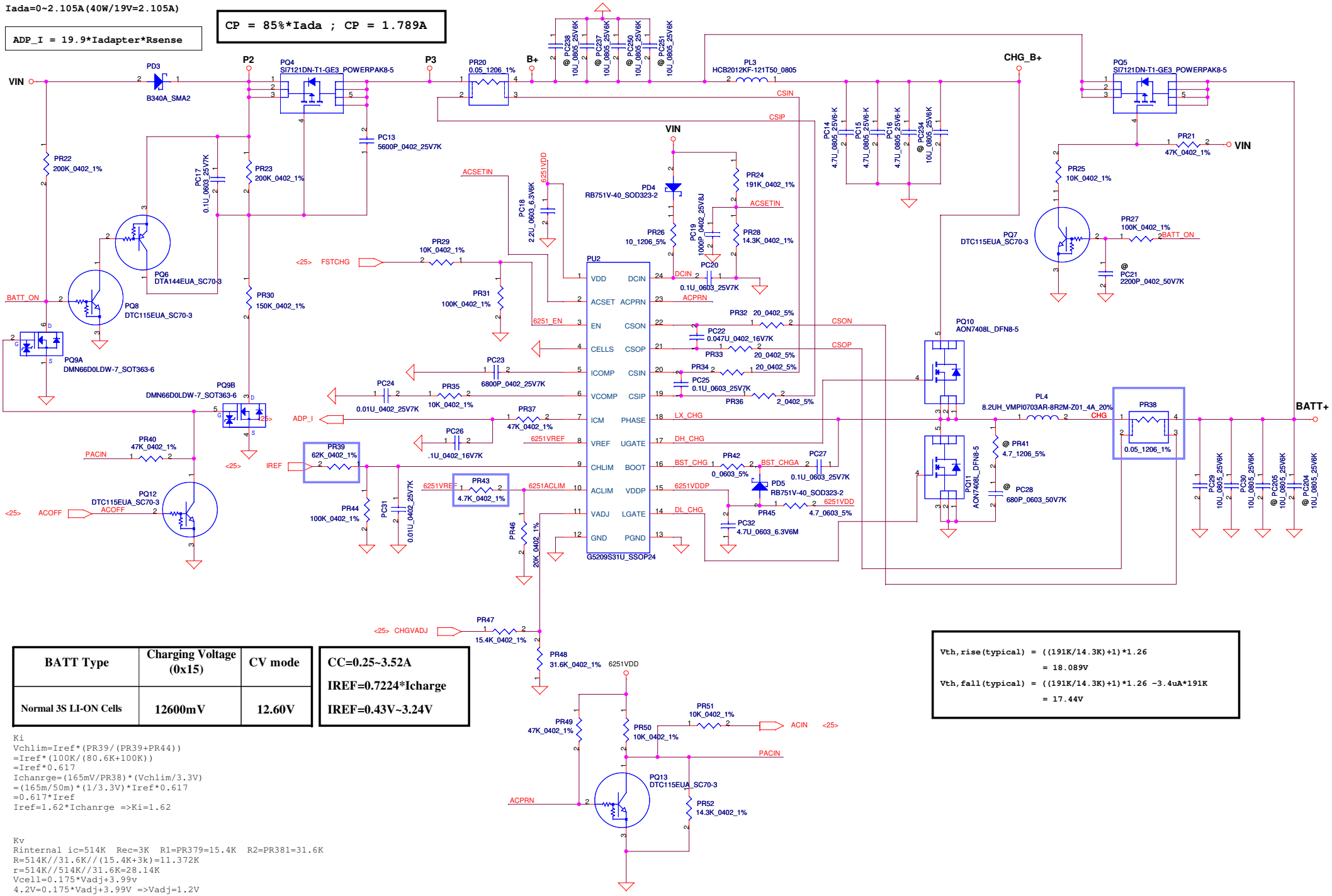
Size	Document Number	Rev
		1.0

Date: Wednesday, November 17, 2010 | Sheet 29 of 36

Iada=0~2.105A(40W/19V=2.105A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 1.789A



BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.25~3.52A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

```
Vth,rise(typical) = ((191K/14.3K)+1)*1.26
                  = 18.089V
Vth,fall(typical) = ((191K/14.3K)+1)*1.26 -3.4uA*191K
                  = 17.44V
```

Ki
Vchlim=Iref*(PR39/(PR39+PR44))
=Iref*(100K/(80.6K+100K))
=Iref*0.617
Ichanrge=(165mV/PR38)*(Vchlim/3.3V)
=(165m/50m)*(1/3.3V)*Iref*0.617
=0.617*Iref
Iref=1.62*Ichanrge =>Ki=1.62

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

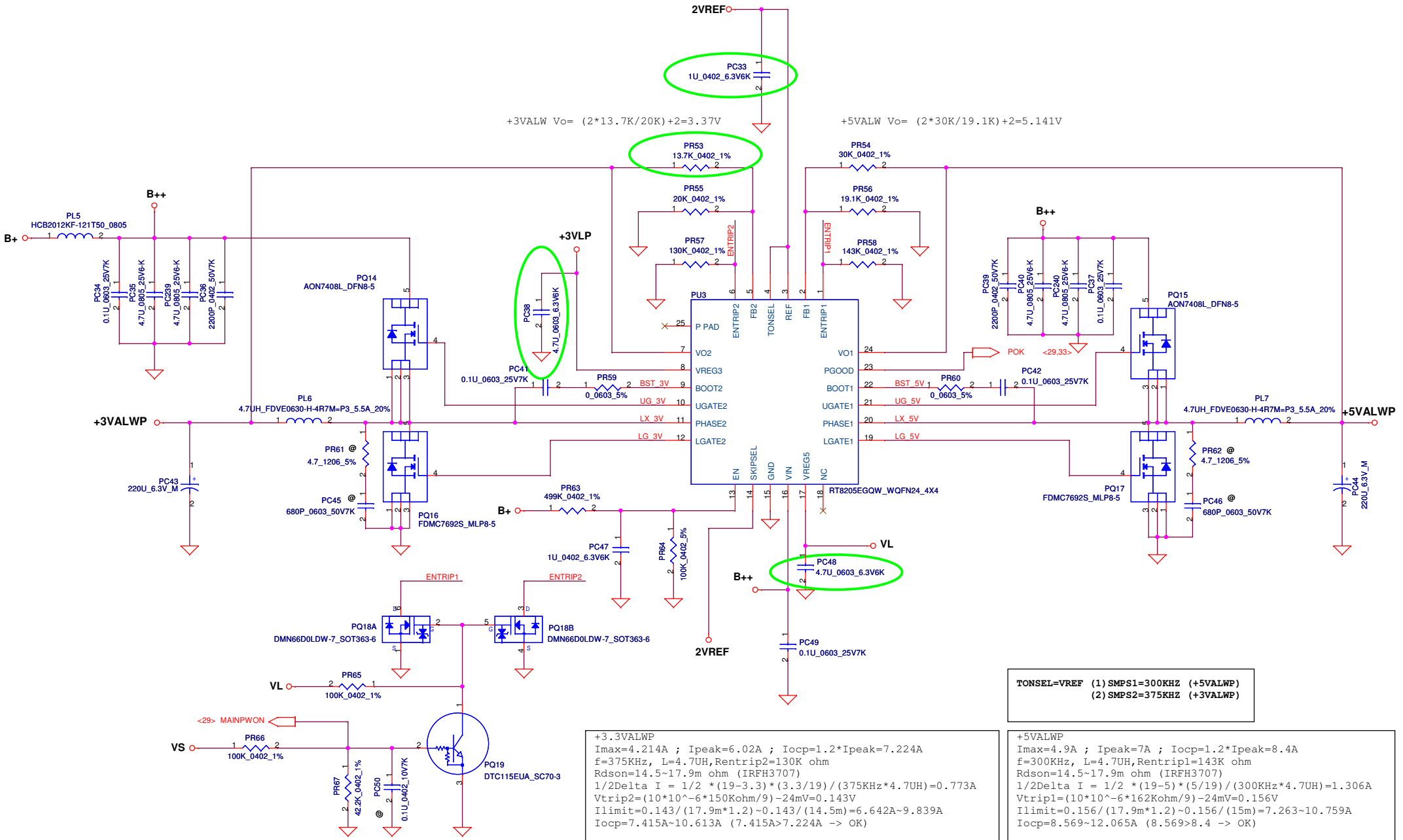
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		1.0

Date: Wednesday, November 17, 2010 | Sheet 30 of 36



TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ (+3VALWP)

+3.3VALWP
Imax=4.214A ; Ipeak=6.02A ; Iocp=1.2*Ipeak=7.224A
f=375KHz, L=4.7UH,Rentrip2=130K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 *(19-3.3)*(3.3/19)/(375KHz*4.7UH)=0.773A
Vtrip2=(10*10^-6*150Kohm/9)-24mV=0.143V
Ilimit=0.143/(17.9m*1.2)~0.143/(14.5m)=6.642A~9.839A
Iocp=7.415A~10.613A (7.415A>7.224A -> OK)

+5VALWP
Imax=4.9A ; Ipeak=7A ; Iocp=1.2*Ipeak=8.4A
f=300KHz, L=4.7UH,Rentrip1=143K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 *(19-5)*(5/19)/(300KHz*4.7UH)=1.306A
Vtrip1=(10*10^-6*162Kohm/9)-24mV=0.156V
Ilimit=0.156/(17.9m*1.2)~0.156/(15m)=7.263~10.759A
Iocp=8.569~12.065A (8.569>8.4 -> OK)

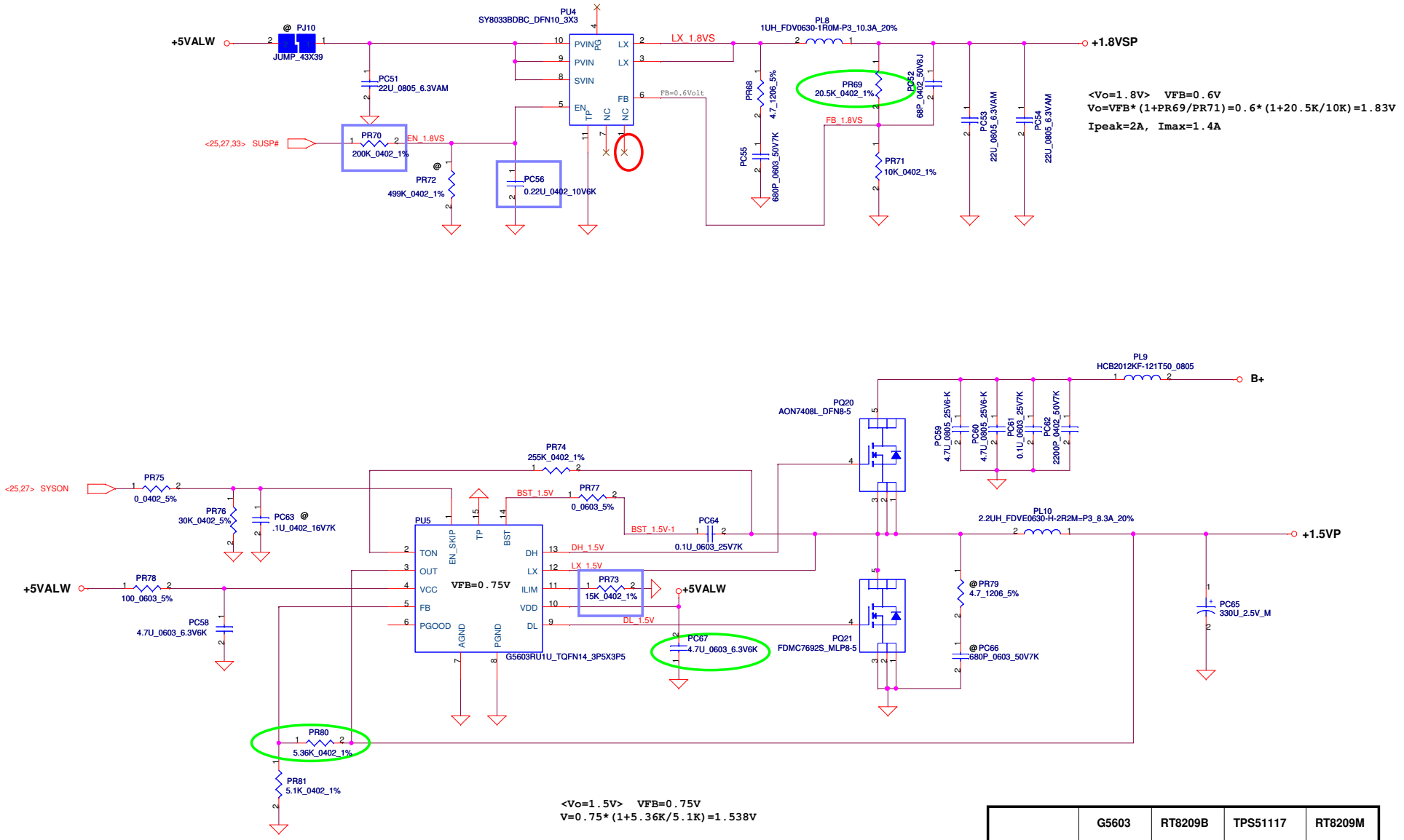
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
	1.0	

Date: Wednesday, November 17, 2010 Sheet 31 of 36



	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

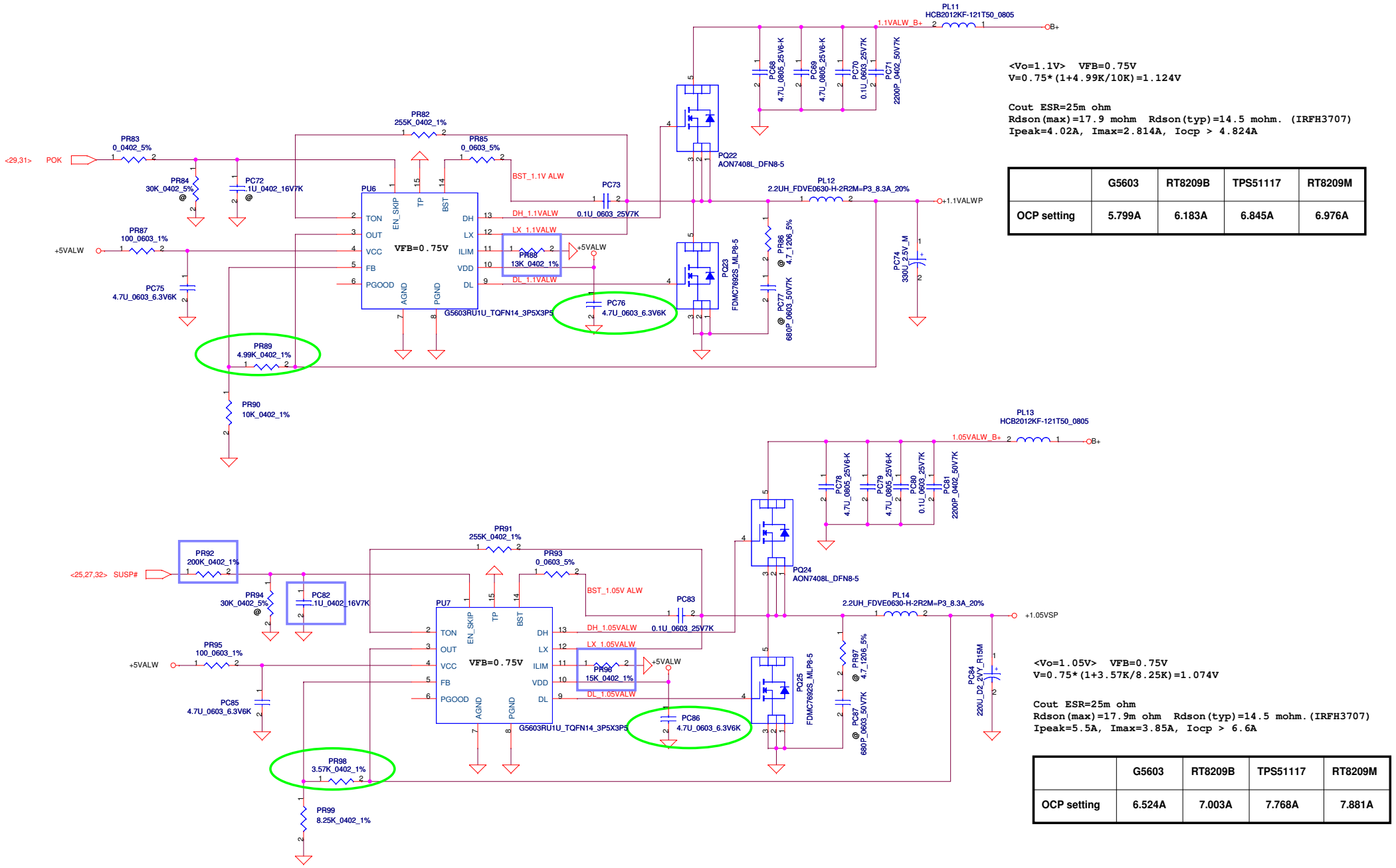
	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Compal Electronics, Inc.

Title: 1.8VSP/1.5VP

Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 32 of 36



	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

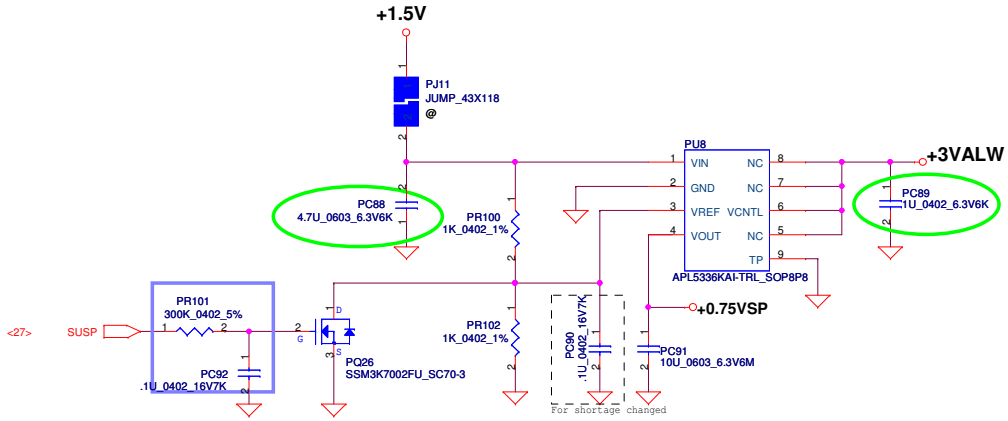
	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Compal Electronics, Inc.

Title: 1.1VALWP/1.0VSP

Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, November 17, 2010 | Sheet 33 of 36



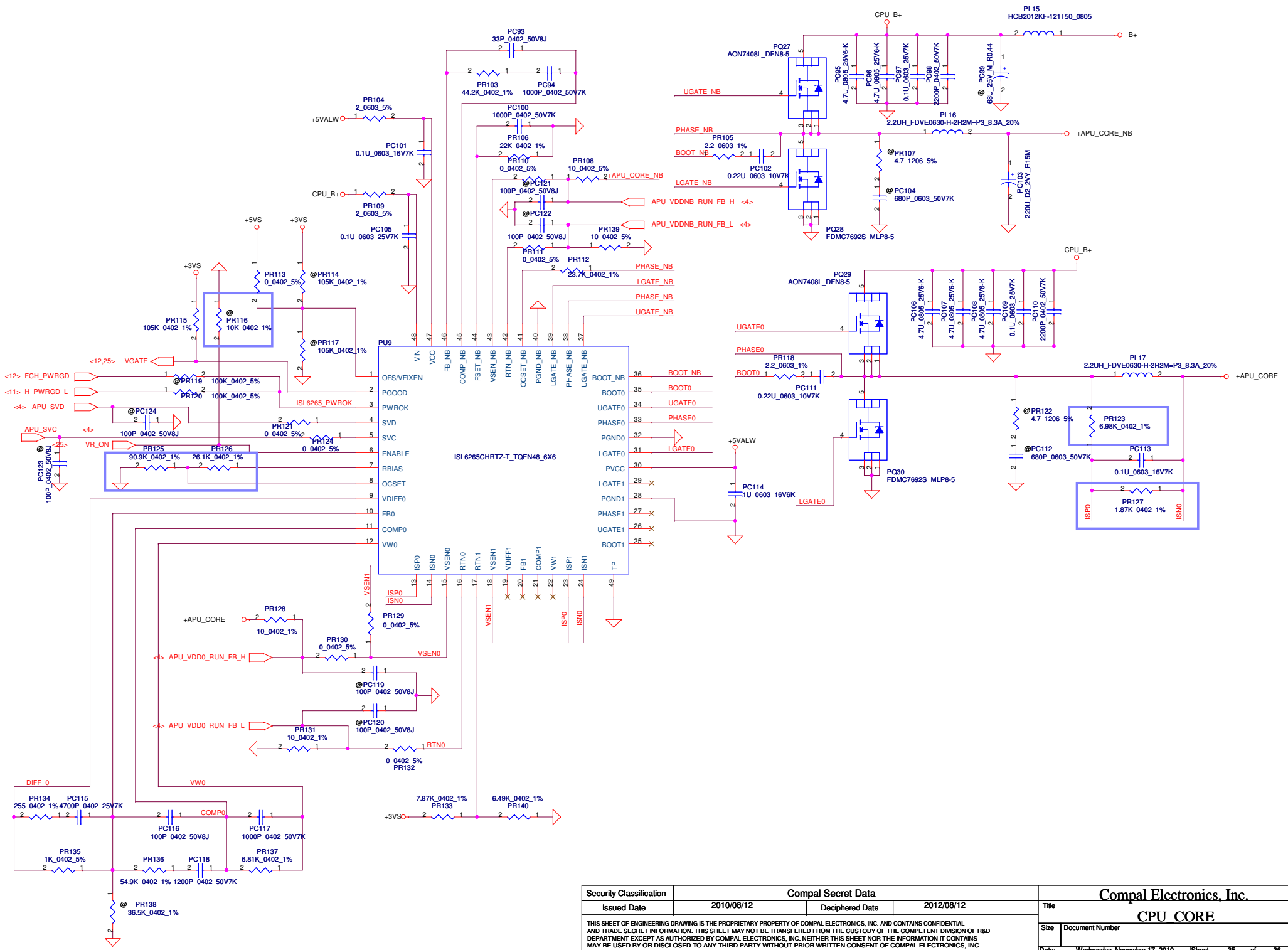
Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: 0.75VSP

Size	Document Number	Rev
		1.0

Date: Wednesday, November 17, 2010 | Sheet 34 of 36



Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: CPU_CORE

Size | Document Number | Rev 1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify CP point for 40W adapter (40W*0.85=34W)	1	30	Change PR43 from SD034249280 (S RES 1/16W 24.9K +-1% 0402) to SD034470180 (S RES 1/16W 4.7K +-1% 0402)	20101011	EVT
2		Modify Outpot current sensor follow PAV70 design	1	30	Change PR38 from SD012200D80 (S RES 1/2W 0.02 +-1% 1206) to SD00000CI10 (S RES 1/2W 0.05 +-1% 1206)	20101011	EVT
3		Modify KI =1.62 follow PAV70 design	1	30	Change PR39 from SD034309380 (S RES 1/16W 309K +1% 0402) to SD034620280 (S RES 1/16W 62K +-1% 0402)	20101011	EVT
4		Modify 1.5V OCP (there is only one dimm for 10.1")	1	32	Change PR73 from SD034787180 (S RES 1/16W 7.87K +-1% 0402) to SD034150280 (S RES 1/16W 15K +-1% 0402)	20101011	EVT
5		Modify 1.1V OCP for G5603	1	33	Change PR88 from SD034100280 (S RES 1/16W 10K +-1% 0402) to SD034130280 (S RES 1/16W 13K +-1% 0402)	20101011	EVT
6		Modify 1.05V OCP for G5603	1	33	Change PR96 from SD034140280 (S RES 1/16W 14K +-1% 0402) to SD034150280 (S RES 1/16W 15K +-1% 0402)	20101011	EVT
7		Modify +APU CORE OCP setting	1	35	Change PR123 to 6.98K ohm , PR127 to 1.87K ohm, PR125 to 90.9K ohm, PR126 to 26.1K ohm	20101011	EVT
8		+APU CORE power sequence concern	1	35	change PR116 to non-pop	20101011	EVT
9		Modify RTC schematic	1	28	add PR141 & PR142 =560 ohm	20101011	EVT
10		Modify SY8033B Enable pin pull down resistor	1	32	Change PR72 to non-pop	20101011	EVT
11		Modify 1.8VS power sequence	1	32	Change PR70 to 200K ohm , add PC56 =0.22uF	20101012	EVT
12		Modify 1.05VSP power sequence	1	33	Change PR92 to 200K ohm , add PC82 =0.1uF	20101012	EVT
13		Modify 0.75VSP power sequence	1	34	Change PR101 to 300K ohm , add PC92 =0.1uF	20101012	EVT
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

Security Classification	Compal Secret Data		
Issued Date	2010/08/12	Deciphered Date	2012/08/12

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom		1.0

Date: Monday, November 15, 2010 | Sheet 36 of 36